Figure 4-3 Synchronous Clocked Sequential Circuit

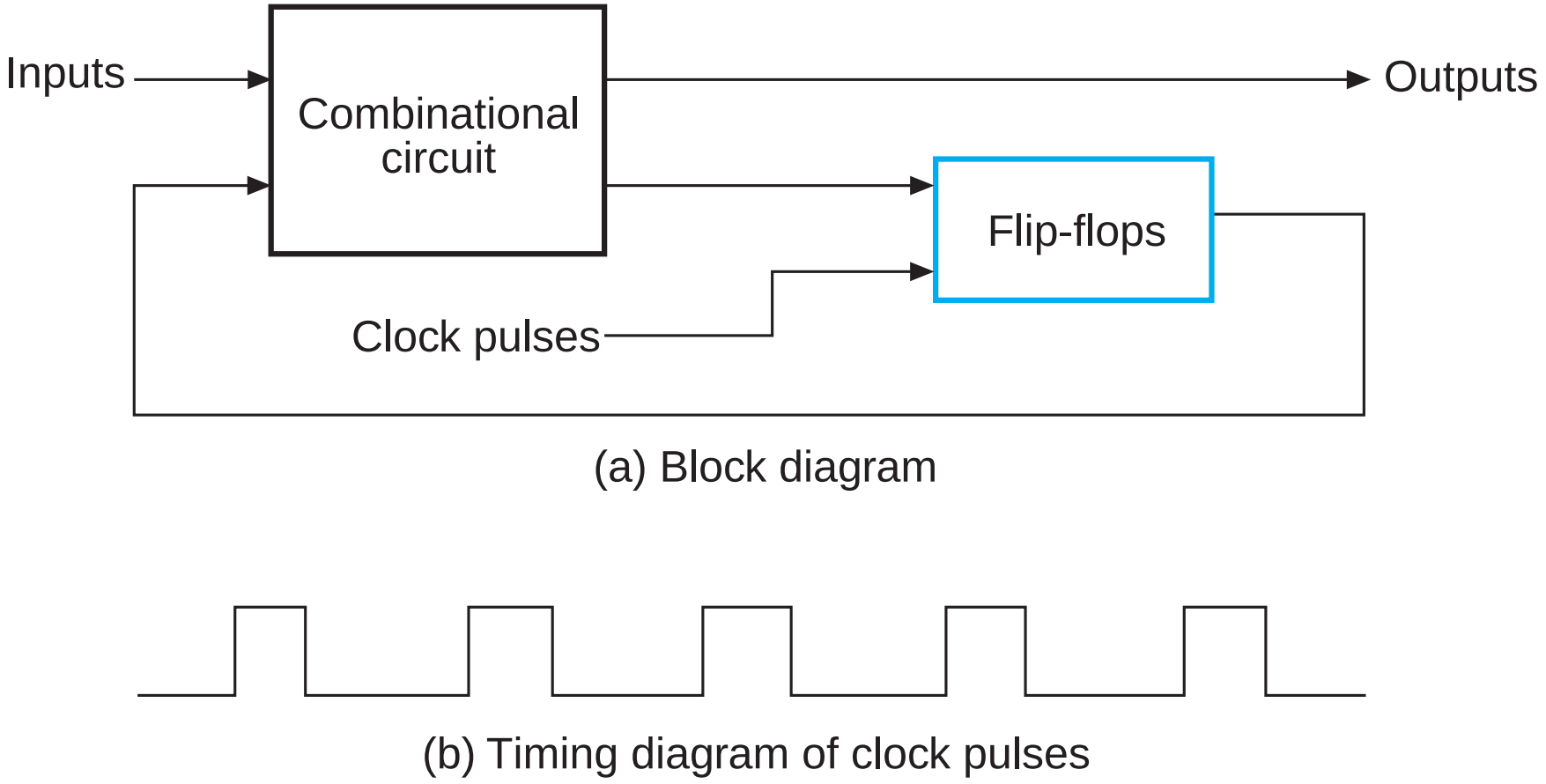


Table 4-1 Flip-Flop Characteristic Table

(a) *JK* Flip-Flop

J	K	$Q(t+1)$	Operation
0	0	$Q(t)$	No change
0	1	0	Reset
1	0	1	Set
1	1	$\overline{Q}(t)$	Complement

(b) *SR* Flip-Flop

S	R	$Q(t+1)$	Operation
0	0	$Q(t)$	No change
0	1	0	Reset
1	0	1	Set
1	1	?	Undefined

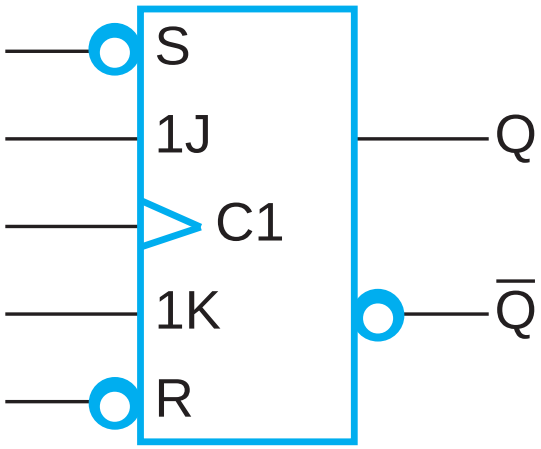
(c) *D* Flip-Flop

D	$Q(t+1)$	Operation
0	0	Reset
1	1	Set

(d) *T* Flip-Flop

T	$Q(t+1)$	Operation
0	$Q(t)$	No change
1	$\overline{Q}(t)$	Complement

Figure 4-16 *JK* Flip-Flop with Direct Set and Reset



(a) Graphic symbols

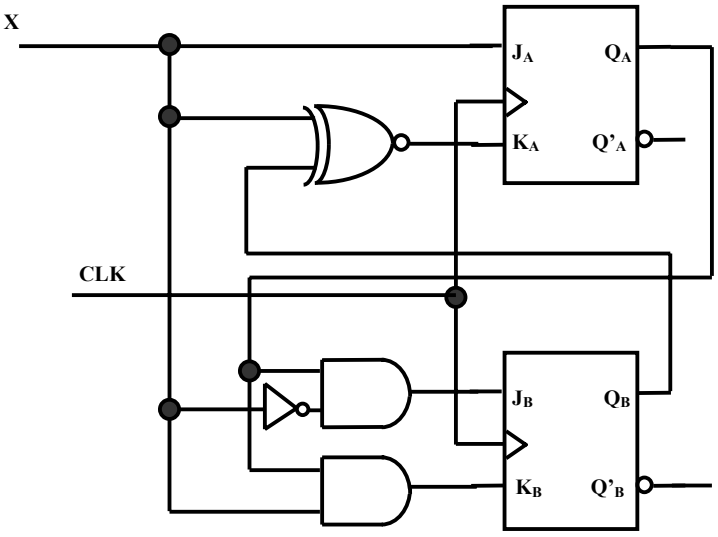
S	R	C	J	K	Q	$\overline{Q}$
0	1	X	X	X	1	0
1	0	X	X	X	0	1
0	0	X	X	X	Undefined	
1	1	↑	0	0	No change	
1	1	↑	0	1	0	1
1	1	↑	1	0	1	0
1	1	↑	1	1	Complement	

(b) Function table

Analysis Procedure:

1. **Obtain flip-flop input equations**
2. **Write down characteristic table of each type of flip-flop in use**
3. **Develop state table**
4. **Obtain state diagram**

- **Example #1:**



Step 1: Flip-flop input equations and output equation

$J_A = X$
$K_A = \overline{Q_B \oplus X} = Q_B \odot X$
$J_B = Q_A X'$
$K_B = Q_A X$

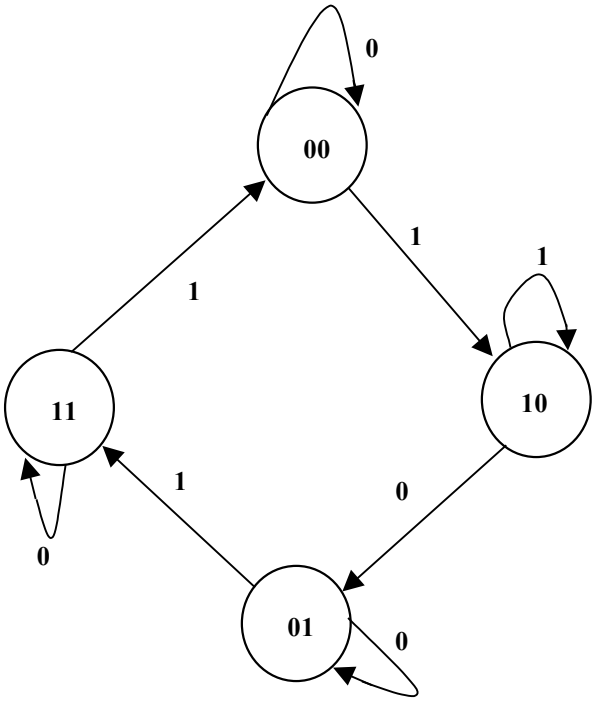
Step 2: Characteristic Table

J K	Q(t+1)
0 0	Q(t)
0 1	0
1 0	1
1 1	Q'(t)

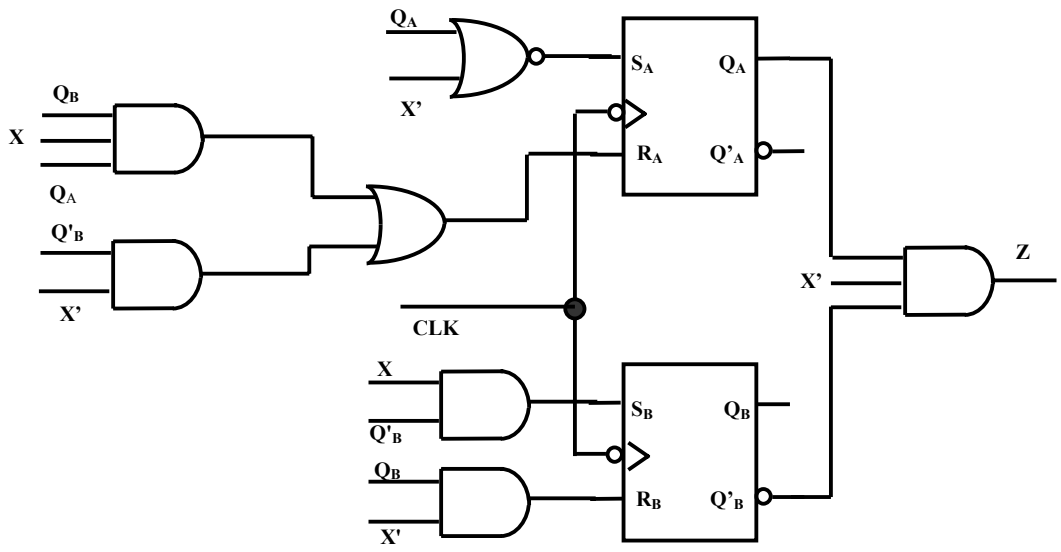
Step 3: State Table

PS $Q_A Q_B$ X	J_A	K_A	J_B	K_B	NS $Q_A Q_B$
000	**0**	**1**	**0**	**0**	**0 0**
001	**1**	**0**	**0**	**0**	**1 0**
010	**0**	**0**	**0**	**0**	**0 1**
011	**1**	**1**	**0**	**0**	**1 1**
100	**0**	**1**	**1**	**0**	**0 1**
101	**1**	**0**	**0**	**1**	**1 0**
110	**0**	**0**	**1**	**0**	**1 1**
111	**1**	**1**	**0**	**1**	**0 0**

Step 4: State Diagram



- **Example #2:**



Step 1: Flip-flop input equations and output equation

$S_A = (Q_A + X')' = Q'_A X$
$R_A = Q_A Q_B X + Q'_B X'$
$S_B = Q'_B X$
$R_B = Q_B X'$
$Z = Q_A Q'_B X'$

Step 2: Characteristic Table

S R	Q(t+1)
0 0	Q(t)
0 1	0
1 0	1
1 1	-

Step 3: State Table

PS $Q_A Q_B$ X	S_A	R_A	S_B	R_B	NS $Q_A Q_B$	Z
000	0	1	0	0	0 0	0
001	1	0	1	0	1 1	0
010	0	0	0	1	0 0	0
011	1	0	0	0	1 1	0
100	0	1	0	0	0 0	1
101	0	0	1	0	1 1	0
110	0	0	0	1	1 0	0
111	0	1	0	0	0 1	0

Step 4: State Diagram

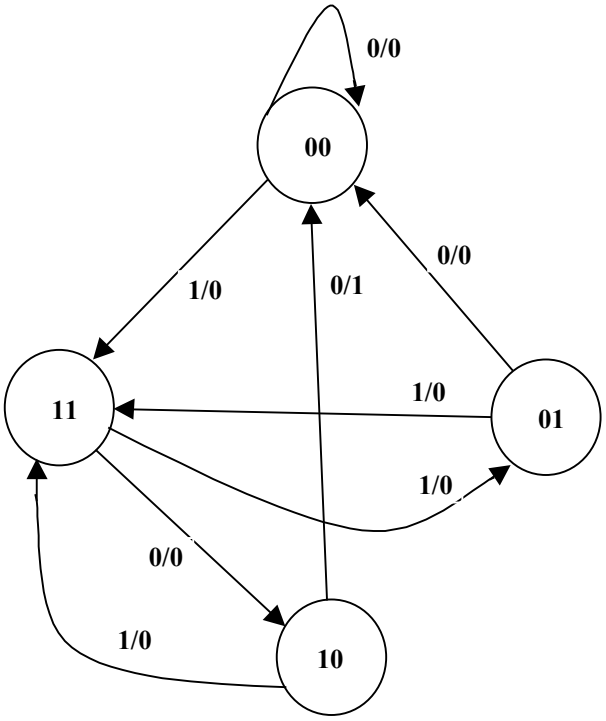
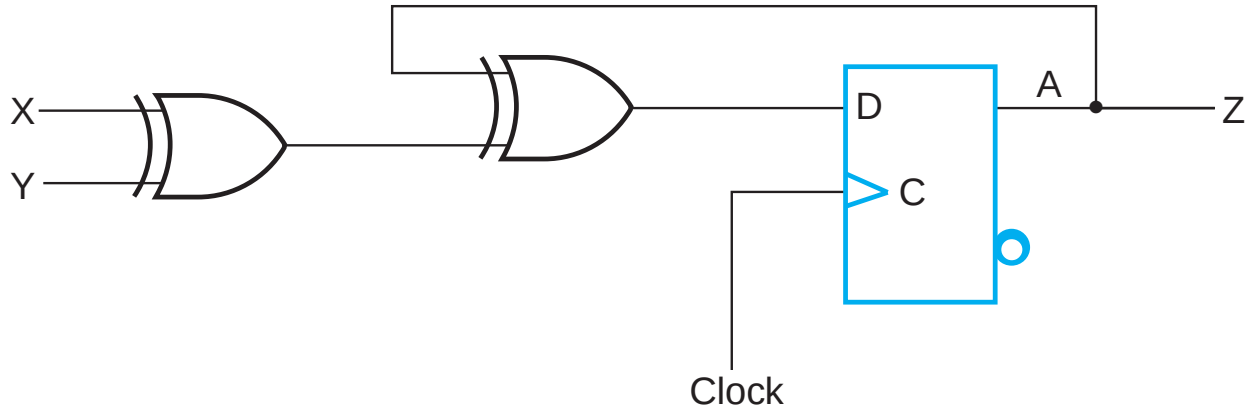


Figure 4-19 Logic Diagram and State Table for $D_A = A \oplus X \oplus Y$

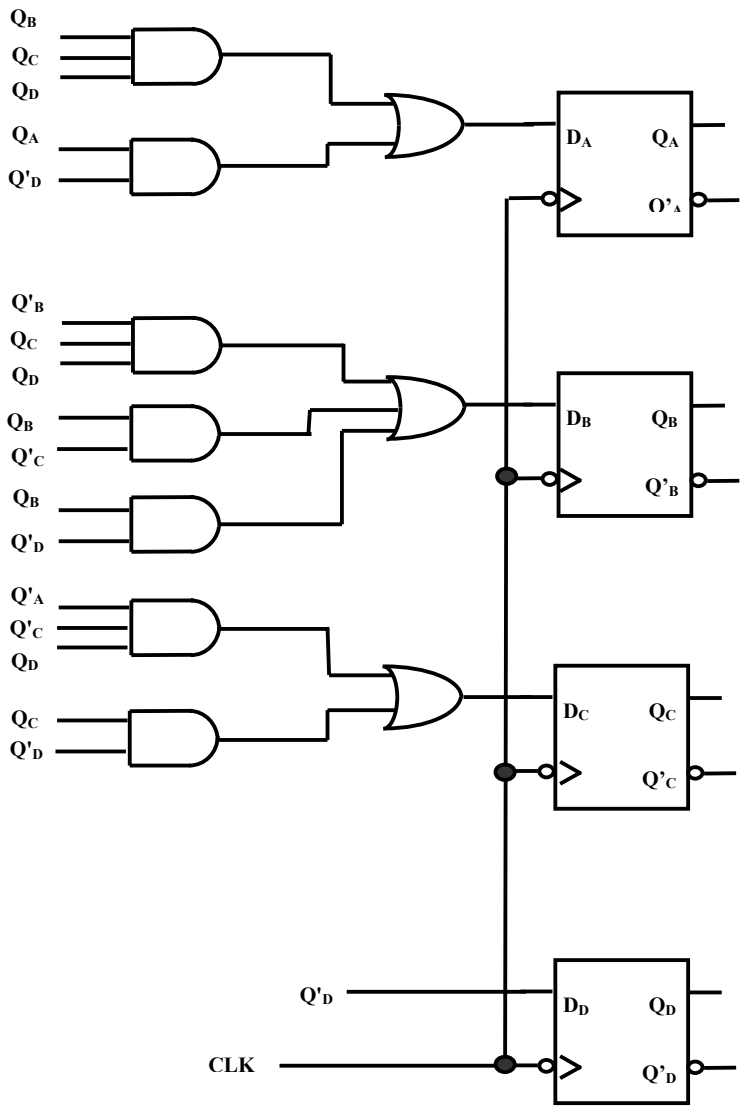


(a)

Present state	Inputs		Next state	Output
A	X	Y	A	Z
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	0
1	0	0	1	1
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

(b) State table

❑ Example #3:



Step 1: Flip-flop input equations

$D_A = Q_B Q_C Q_D + Q_A Q_D'$
$D_B = Q_B' Q_C Q_D + Q_B Q_C' + Q_B Q_D'$
$D_C = Q_A' Q_C' Q_D + Q_C Q_D'$
$D_D = Q_D'$

Step 2: Characteristic Table

D	Q(t+1)
0	0
1	1

Step 3: State Table

PS $Q_AQ_BQ_CQ_D$	D_A	D_B	D_C	D_D	NS $Q_AQ_BQ_CQ_D$
0 0 0 0	0	0	0	1	0 0 0 1
0 0 0 1	0	0	1	0	0 0 1 0
0 0 1 0	0	0	1	1	0 0 1 1
0 0 1 1	0	1	0	0	0 1 0 0
0 1 0 0	0	1	0	1	0 1 0 1
0 1 0 1	0	1	1	0	0 1 1 0
0 1 1 0	0	1	1	1	0 1 1 1
0 1 1 1	1	0	0	0	1 0 0 0
1 0 0 0	1	0	0	1	1 0 0 1
1 0 0 1	0	0	0	0	0 0 0 0
1 0 1 0	1	0	1	1	1 0 1 1
1 0 1 1	0	1	0	0	0 1 0 0
1 1 0 0	1	1	0	1	1 1 0 1
1 1 0 1	0	1	0	0	0 1 0 0
1 1 1 0	1	1	1	1	1 1 1 1
1 1 1 1	1	0	0	0	1 0 0 0

Step 4: State Diagram

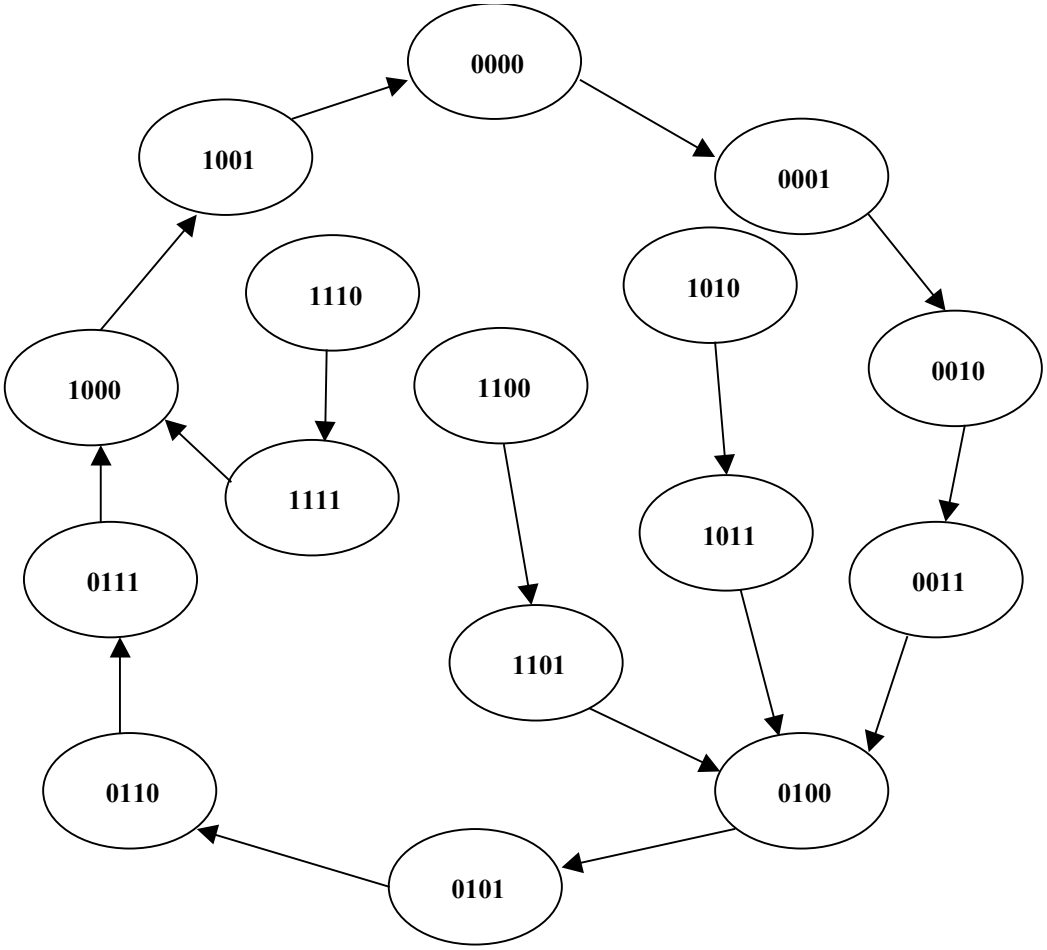


Table 4-10 Flip-Flop Excitation Table

(a) *JK* Flip-Flop

$Q(t)$	$Q(t+1)$	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

(b) *SR* Flip-Flop

$Q(t)$	$Q(t+1)$	S	R
0	0	0	X
0	1	1	0
1	0	0	1
1	1	X	0

(c) *D* Flip-Flop

$Q(t)$	$Q(t+1)$	D
0	0	0
0	1	1
1	0	0
1	1	1

(d) *T* Flip-Flop

$Q(t)$	$Q(t+1)$	T
0	0	0
0	1	1
1	0	1
1	1	0