Xilinx VHDL

<Release Version: 10.1i>

Tutorial

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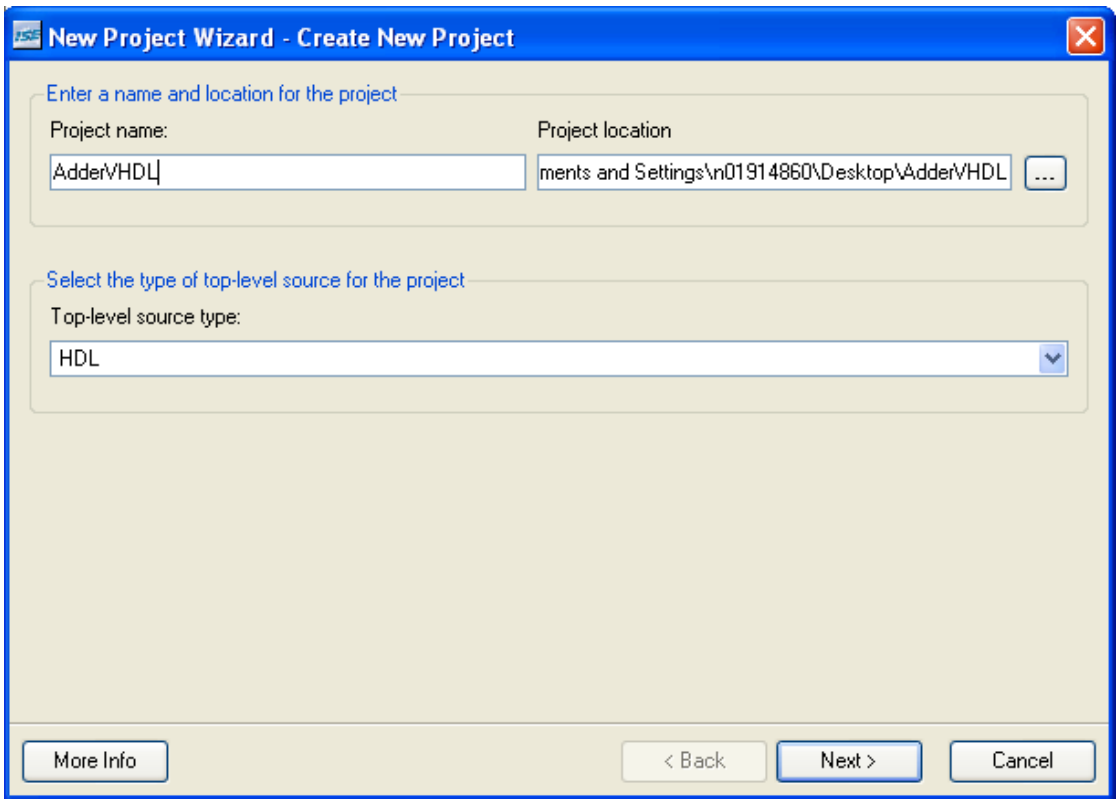
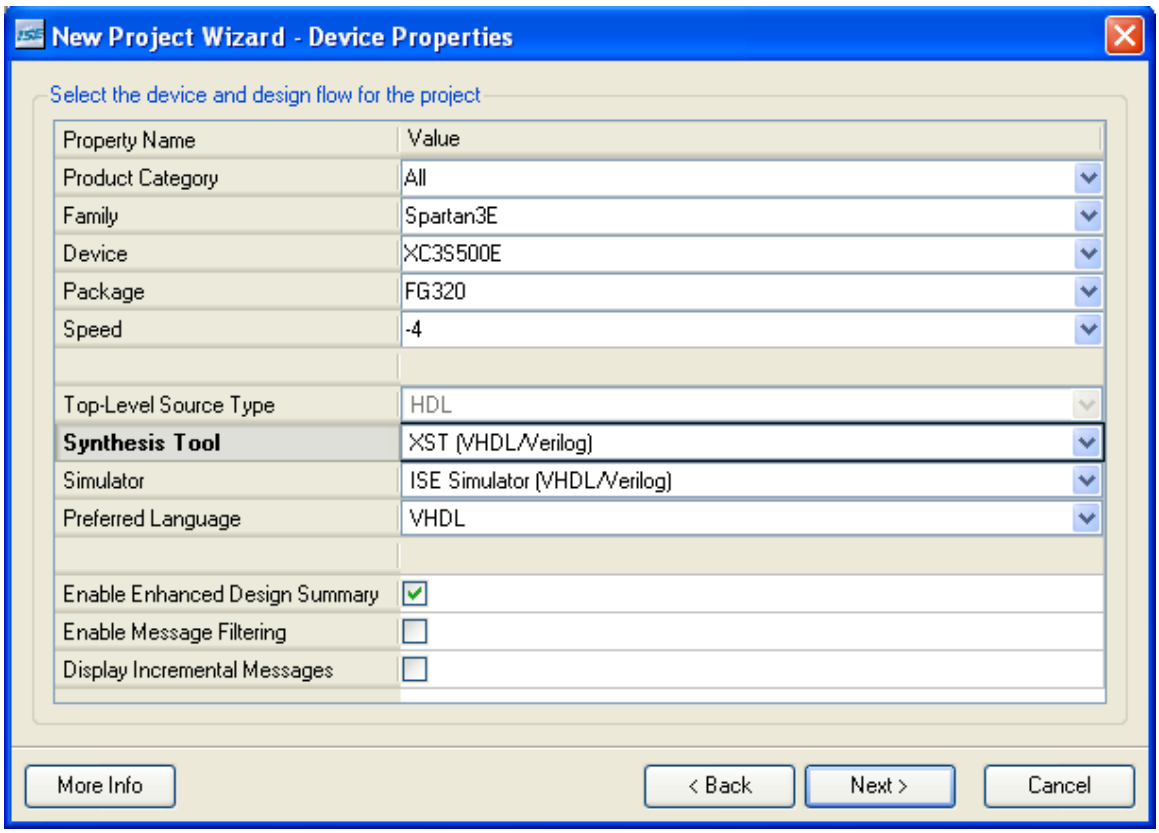
Start A New Project.

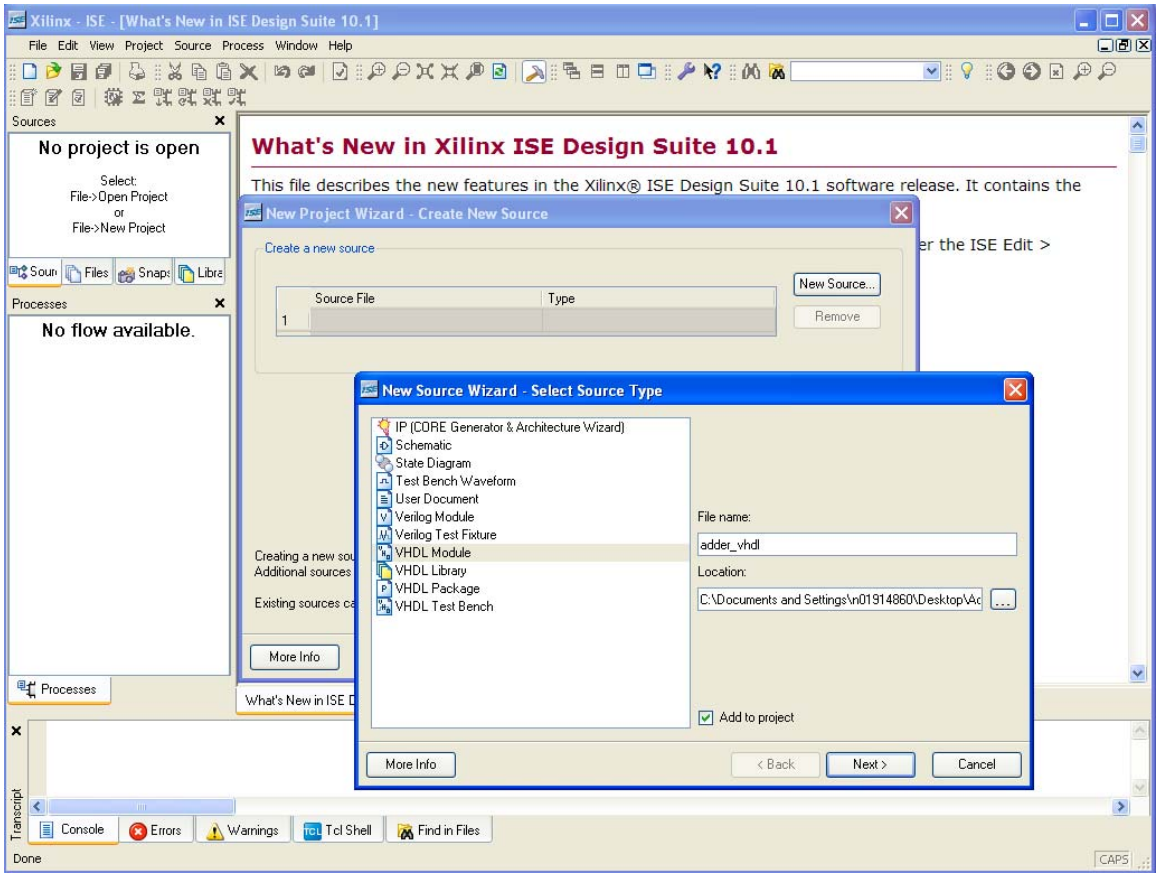


Click Next.

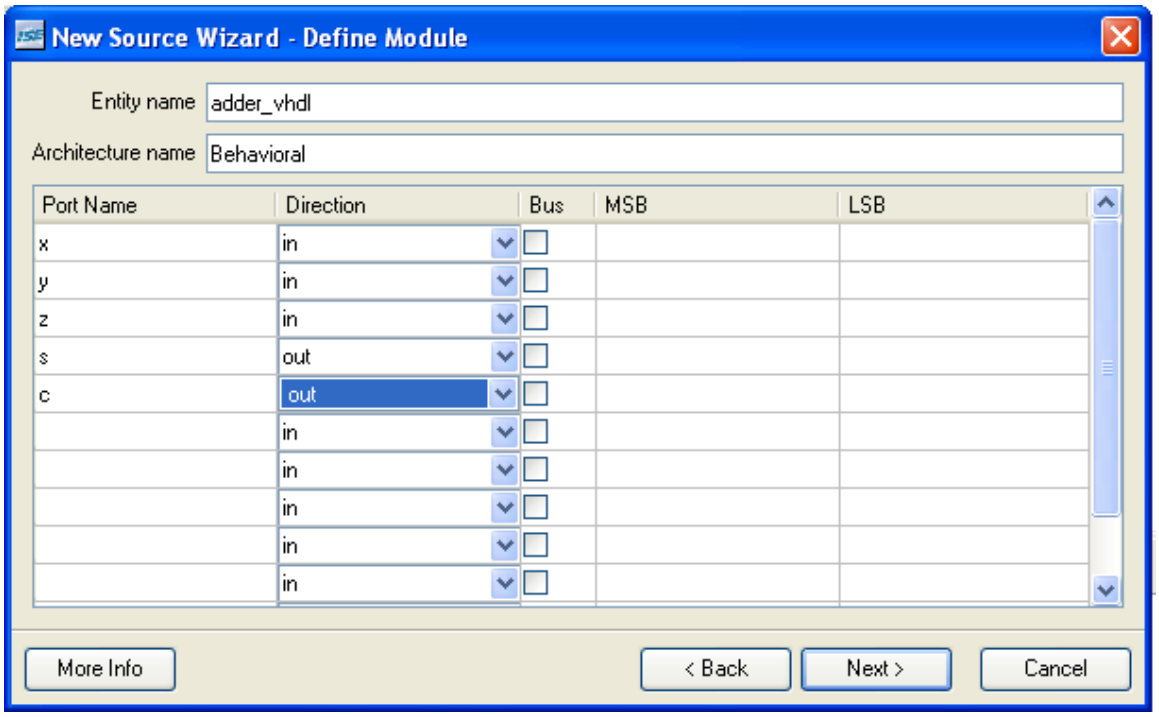
Make Sure the Device Properties are chosen as shown below.



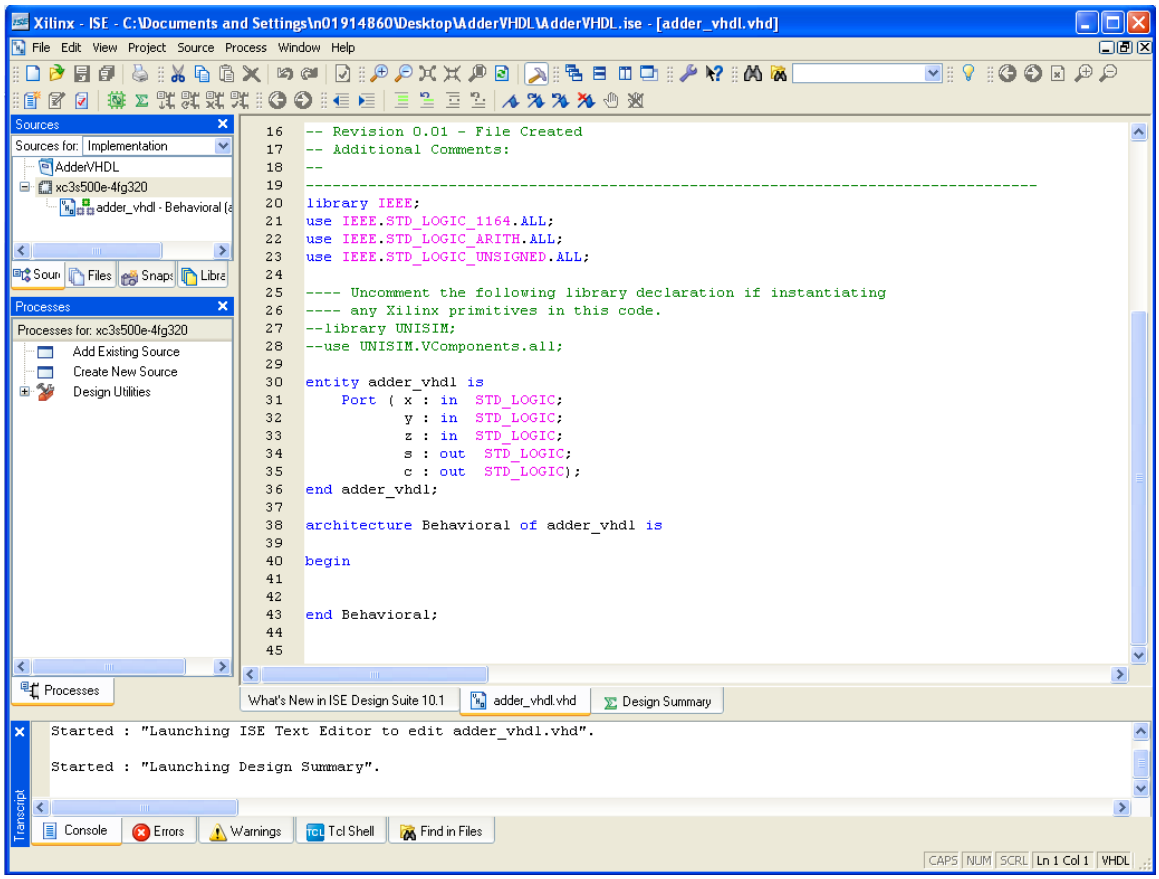
Click Next.
On the New Project Wizard, click on New Source. In New Source Wizard, select VHDL module and type in a filename.



Click “Next”. In this exercise, you are designing a full adder with x, y, and z as inputs and s and c as outputs. Hence, set the ports accordingly and click Next.



Click “Next”, “Next” and “Finish”. This will open a editor where you can input your VHDL code.



Note that

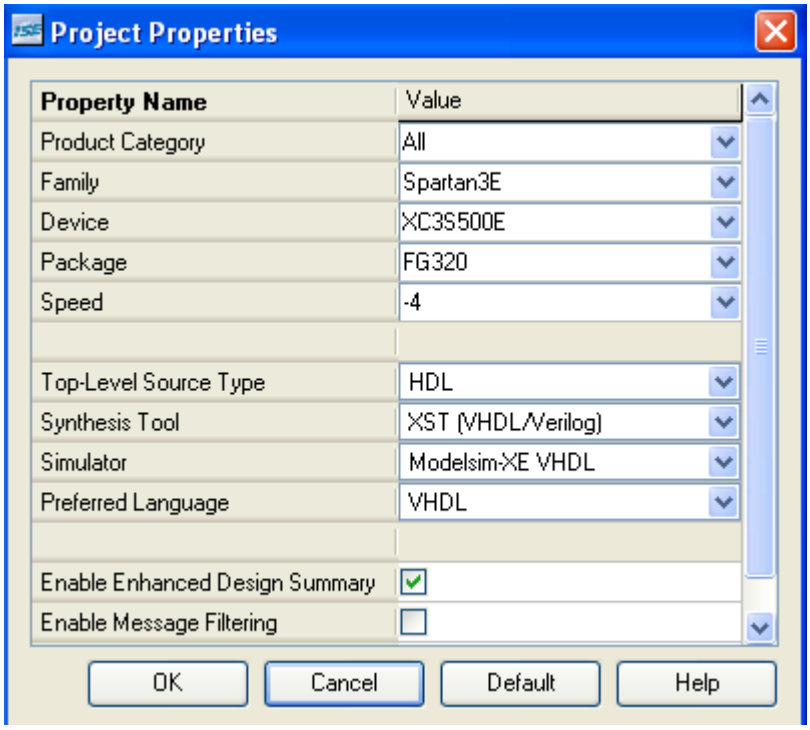
$S = X \oplus Y \oplus Z$
$C = XY + YZ + XZ$

Hence,

```
19  ----------------------------------------------------------------------------
20  library IEEE;
21  use IEEE.STD_LOGIC_1164.ALL;
22  use IEEE.STD_LOGIC_ARITH.ALL;
23  use IEEE.STD_LOGIC_UNSIGNED.ALL;
24
25  ---- Uncomment the following library declaration if instantiating
26  ---- any Xilinx primitives in this code.
27  --library UNISIM;
28  --use UNISIM.VComponents.all;
29
30  entity addervhdal is
31      Port ( x : in  STD_LOGIC;
32             y : in  STD_LOGIC;
33             z : in  STD_LOGIC;
34             s : out  STD_LOGIC;
35             c : out  STD_LOGIC);
36  end addervhdal;
37
38  architecture Behavioral of addervhdal is
39
40  begin
41
42  s <= x xor y xor z;
43  c <= (x and y) or (y and z) or (x and z);
44
45  end Behavioral;
46
47
```

Save the file.

The project can be simulated using ModelSim or ISE simulator. For ISE simulator details refer the ISE Simulator tutorial. ModelSim simulator follows a similar procedure as outlined in ModelSim tutorial. Try to use ModelSim to simulate your design. To simulate it in ModelSim select device properties as



When the design is completed, open the User Constraints Editor and assign the pins to the correct inputs and outputs. Follow the steps in the Download Tutorial to complete the process.