Xilinx VHDL
<Release Version: 10.1i>
Tutorial

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Start A New Project.

Click Next.

Make Sure the Device Properties are chosen as shown below.
Click Next.
Click “Next”. In this exercise, you are designing a full adder with x, y, and z as inputs and s and c as outputs. Hence, set the ports accordingly and click Next.
Click “Next”, “Next” and “Finish”. This will open a editor where you can input your VHDL code.

Note that

\[ S = X \oplus Y \oplus Z \]
\[ C = XY + YZ + XZ \]

Hence,
Save the file.

The project can be simulated using ModelSim or ISE simulator. For ISE simulator details refer the ISE Simulator tutorial. ModelSim simulator follows a similar procedure as outlined in ModelSim tutorial. Try to use ModelSim to simulate your design. To simulate it in ModelSim select device properties as

```vhdl
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_ARITH.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;

---- Uncomment the following library declaration if instantiating any Xilinx primitives in this code.
library UNISIM;
use UNISIM.VComponents.all;

entity addervhdl is
  Port ( x : in STD_LOGIC;
         y : in STD_LOGIC;
         z : in STD_LOGIC;
         s : out STD_LOGIC;
         c : out STD_LOGIC);
end addervhdl;

architecture Behavioral of addervhdl is
begin
  s <= x xor y xor z;
  c <= (x and y) or (y and z) or (x and z);
end Behavioral;
```
When the design is completed, open the User Constraints Editor and assign the pins to the correct inputs and outputs. Follow the steps in the Download Tutorial to complete the process.