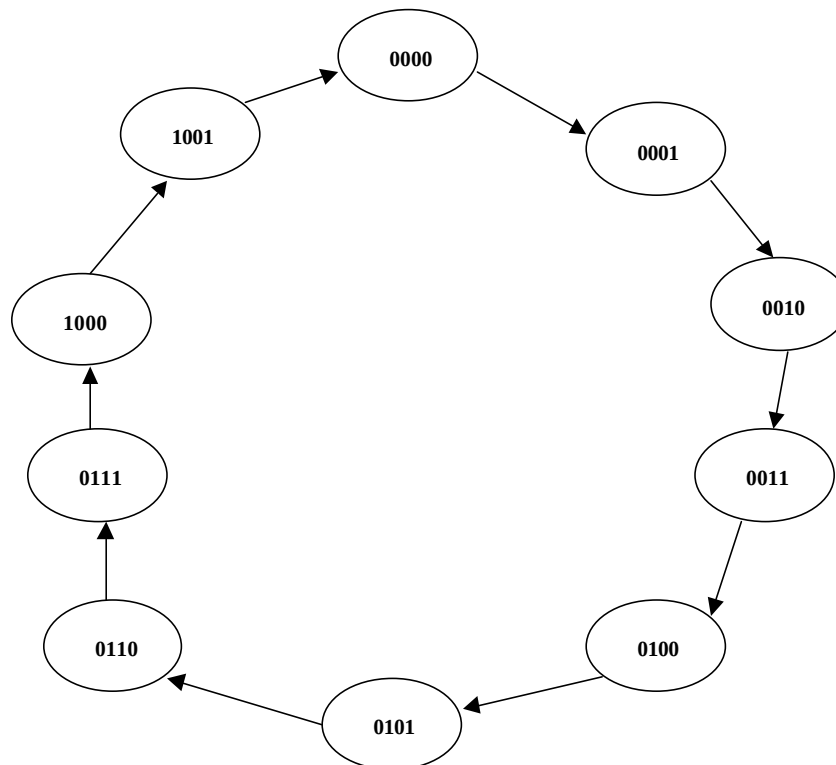


❑ DESIGN PROCEDURE

1. Word description.
2. State diagram.
3. Assign binary values.
4. Decide on type of flip flops.
5. Excitation table for the flip flop.
6. State table.
7. Generate simplified logic equations for flip flop inputs and system outputs.
8. Draw logic diagram.

- ❑ **Example #1: Using D flip-flops, design a 0 to 9 synchronous counter.**

· **State diagram**



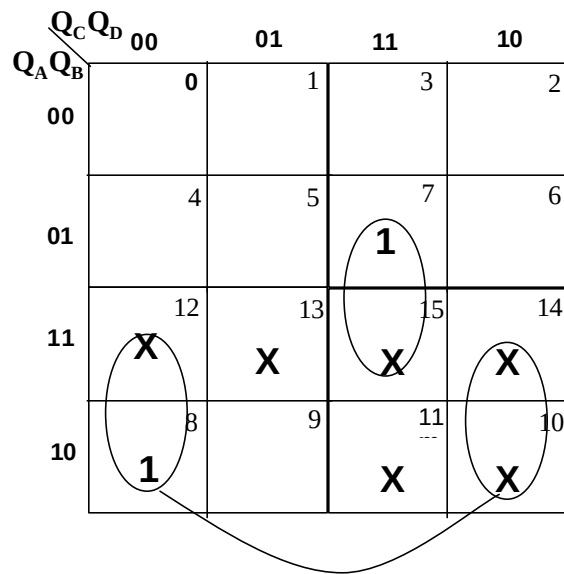
- **D Flip-Flop Excitation Table**

Q(t)	Q(t+1)	D
0	0	0
0	1	1
1	0	0
1	1	1

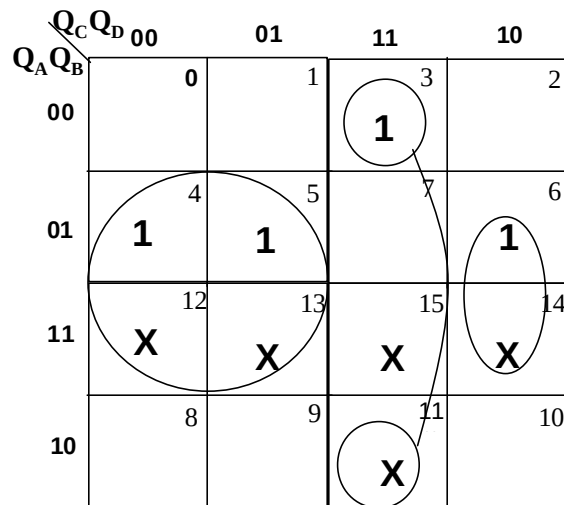
- **State Table**

PRESENT STATE	NEXT STATE				
Q_AQ_BQ_CQ_D	Q_AQ_BQ_CQ_D	D_A	D_B	D_C	D_D
0000	0001	0	0	0	1
0001	0010	0	0	1	0
0010	0011	0	0	1	1
0011	0100	0	1	0	0
0100	0101	0	1	0	1
0101	0110	0	1	1	0
0110	0111	0	1	1	1
0111	1000	1	0	0	0
1000	1001	1	0	0	1
1001	0000	0	0	0	0
1010	XXXX	X	X	X	X
1011	XXXX	X	X	X	X
1100	XXXX	X	X	X	X
1101	XXXX	X	X	X	X
1110	XXXX	X	X	X	X
1111	XXXX	X	X	X	X

• **Karnaugh Map**



• $D_A = Q_B Q_C Q_D + Q_A Q_D'$



• $D_B = Q_B' Q_C Q_D + Q_B Q_C' + Q_B Q_D'$

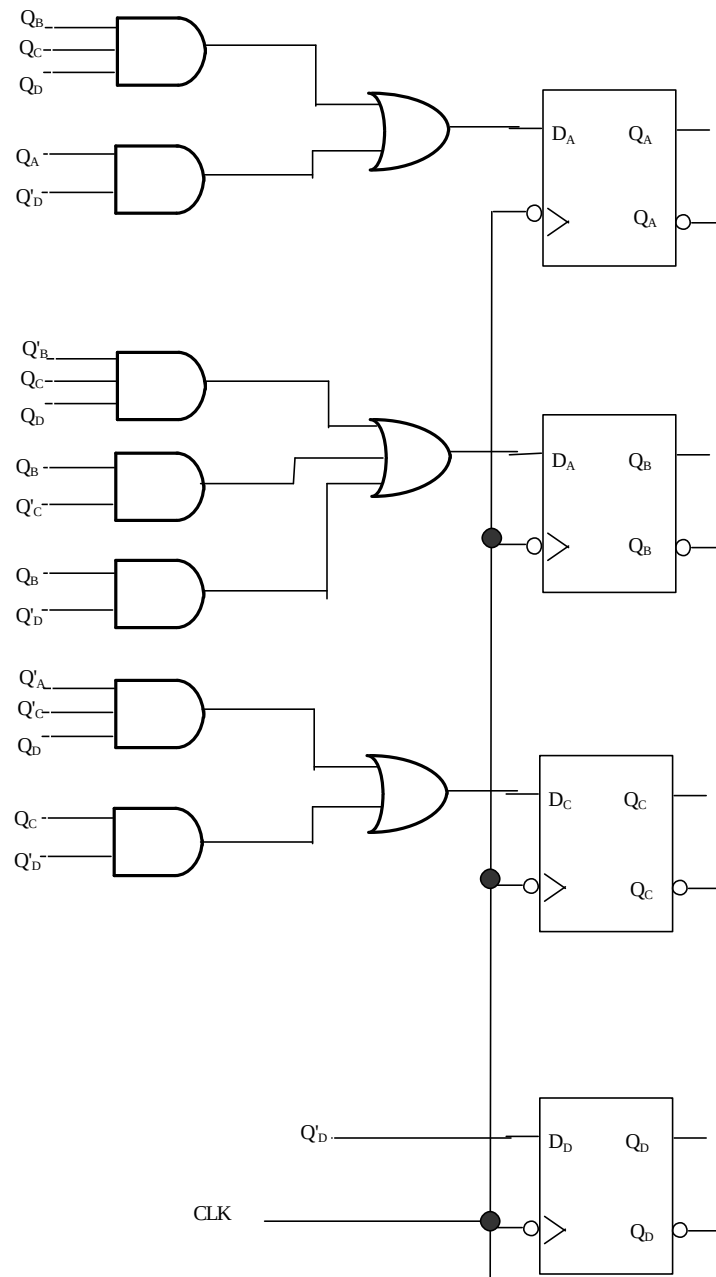
		$Q_C Q_D$			
		00	01	11	10
$Q_A Q_B$	00	0 1	1 1	3	2 1
	01	4	5 1	7	6 1
	11	12 X	13 X	15 X	14 X
	10	8	9	11 X	10 X

· $D_C = Q_A' Q_C' Q_D + Q_C Q_D'$

		$Q_C Q_D$			
		00	01	11	10
$Q_A Q_B$	00	0 1	1	3	2 1
	01	4 1	5	7	6 1
	11	12 X	13 X	15 X	14 X
	10	8 1	9	11 X	10 X

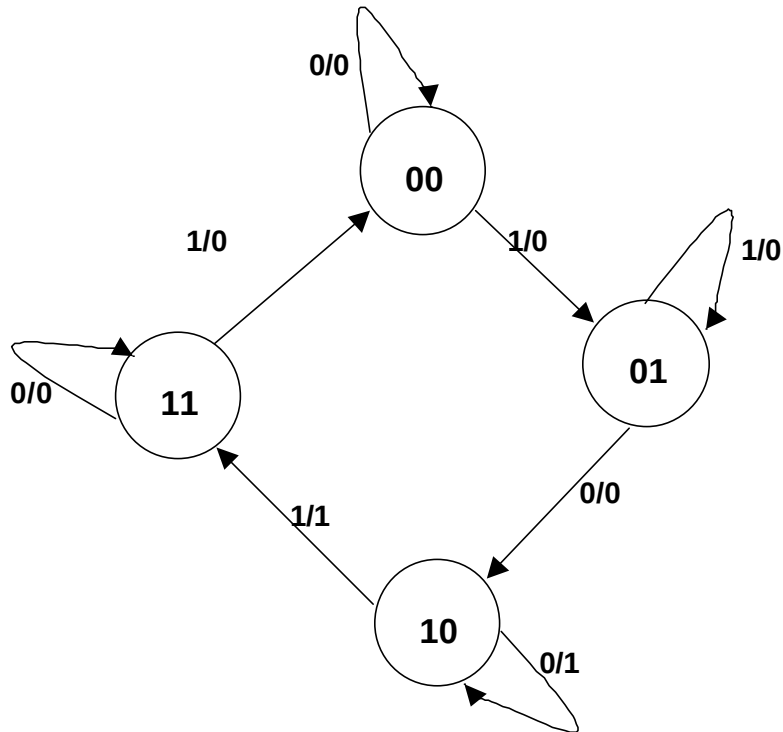
· $D_D = Q_D'$

- **Circuit**



□ **Example #2:**

1. State diagram



2. Use JK flip flops

3. Flip flop Excitation Table

PRESENT STATE	NEXT STATE	J	K
Q(t)	Q(t+1)		
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

4. State Table

PRESENT STATE	INPUT	NEXT STATE	FLIP-FLOP INPUTS				OUTPUT
$Q_A Q_B$	X	$Q_A Q_B$	J_A	K_A	J_B	K_B	Z
00	0	00	0	X	0	X	0
00	1	01	0	X	1	X	0
01	0	10	1	X	X	1	0
01	1	01	0	X	X	0	0
10	0	10	X	0	0	X	1
10	1	11	X	0	1	X	1
11	0	11	X	0	X	0	0
11	1	00	X	1	X	1	0

5. Karnaugh Map

$Q_B \backslash Q_A$	00	01	11	10
0	m_0	m_1	m_3	m_2 1
1	X m_4	X m_5	X m_7	X m_6

• $J_A = Q_B X'$

$Q_B \backslash Q_A$	00	01	11	10
0	X m_0	X m_1	X m_3	X m_2
1	m_4	m_5	1 m_7	m_6

• $K_A = Q_B X$

$Q_B \backslash Q_A$	00	01	11	10
0	m_0	1 m_1	X m_3	X m_2
1	m_4	1 m_5	X m_7	X m_6

· $J_B = X$

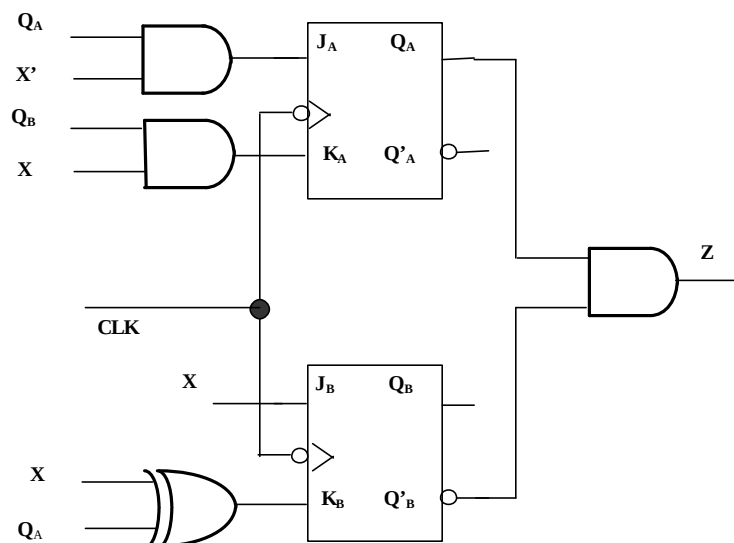
$Q_B \backslash Q_A$	00	01	11	10
0	X m_0	X m_1		1 m_2
1	X m_4	X m_5	1 m_7	

· $K_B = Q_A X' + Q'_A X = Q_A \oplus X$

$Q_B \backslash Q_A$	00	01	11	10
0	m_0	m_1	m_3	m_2
1	1 m_4	1 m_5	m_7	m_6

· $Z = Q_A Q'_B$

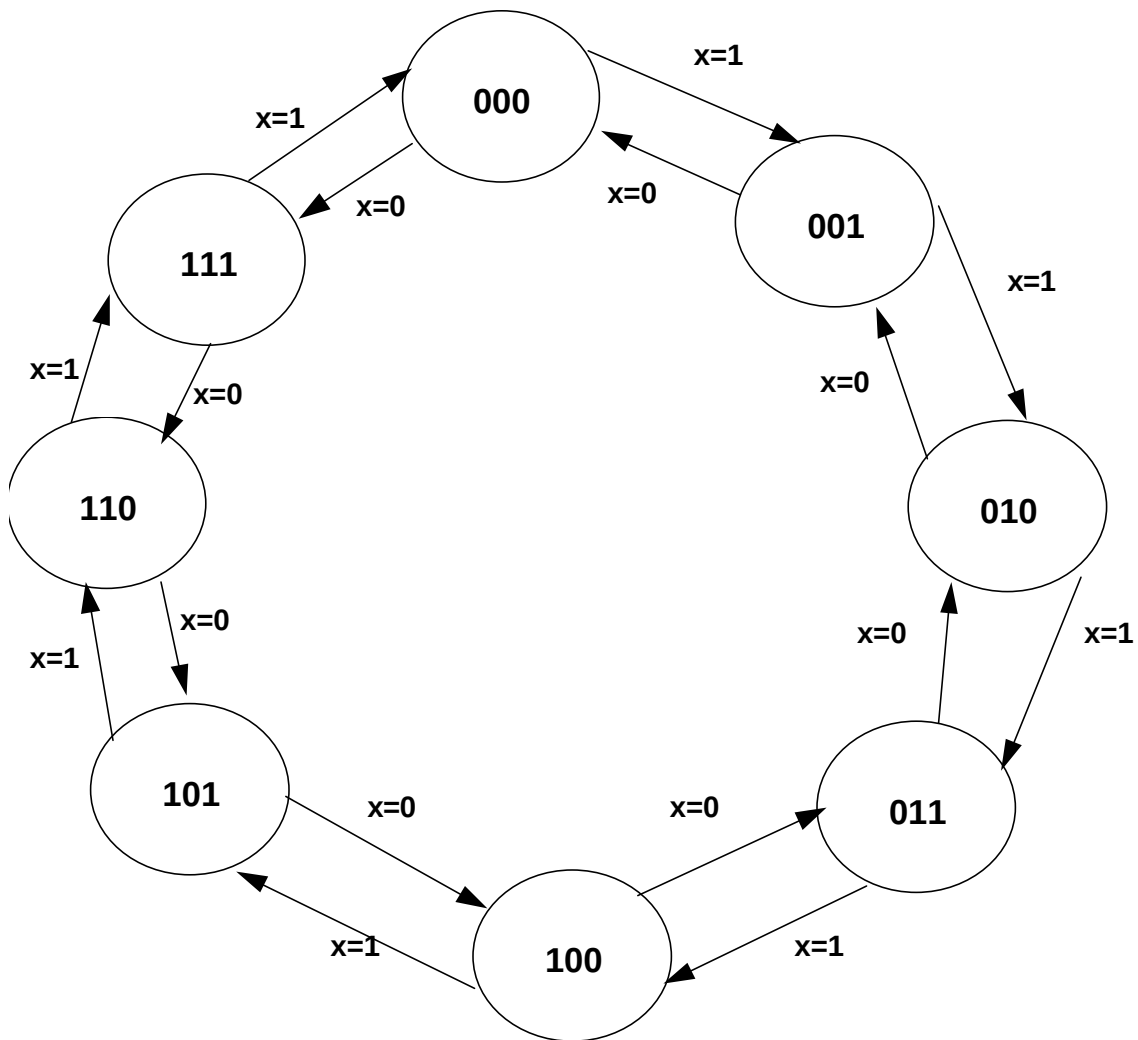
6. Schematic



□ **Example #3:**

Using JK flip-flops, design an up/down synchronous counter as specified below. The counter counts up if input X is 1 and it counts down when X is 0.

• **State Diagram**



- **Use JK flip flops**

- Flip flop Excitation Table

PRESENT STATE	NEXT STATE		
Q(t)	Q(t+1)	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

- State Table

PRESENT STATE	INPUT	NEXT STATE						
Q _A Q _B Q _C	X	Q _A Q _B Q _C	J _A	K _A	J _B	K _B	J _C	K _C
000	0	111	1	X	1	X	1	X
000	1	001	0	X	0	X	1	X
001	0	000	0	X	0	X	X	1
001	1	010	0	X	1	X	X	1
010	0	001	0	X	X	1	1	X
010	1	011	0	X	X	0	1	X
011	0	010	0	X	X	0	X	1
011	1	100	1	X	X	1	X	1
100	0	011	X	1	1	X	1	X
100	1	101	X	0	0	X	1	X
101	0	100	X	0	0	X	X	1
101	1	110	X	0	1	X	X	1
110	0	101	X	0	X	1	1	X
110	1	111	X	0	X	0	1	X
111	0	110	X	0	X	0	X	1
111	1	000	X	1	X	1	X	1

Karnaugh Map

		$Q_C X$			
Q_A	Q_B	00	01	11	10
	00	m_0 1	m_1	m_3	m_2
	01	m_4	m_5	m_7 1	m_6
	11	m_{12} X	m_{13} X	m_{15} X	m_{14} X
	10	m_8 X	m_9 X	m_{11} X	m_{10} X

$$J_A = Q'_B Q'_C X' + Q_B Q_C X$$

		$Q_C X$			
Q_A	Q_B	00	01	11	10
	00	m_0 X	m_1 X	m_3 X	m_2 X
	01	m_4 X	m_5 X	m_7 X	m_6 X
	11	m_{12}	m_{13}	m_{15} 1	m_{14}
	10	m_8 1	m_9	m_{11}	m_{10}

$$K_A = Q'_B Q'_C X' + Q_B Q_C X$$

$Q_A \backslash Q_B \backslash Q_C X$		00	01	11	10
00	1 m_7		m_1	1 m_3	m_2
01	X m_4	X m_5		X m_7	X m_6
11	X m_{12}	X m_{13}		X m_{15}	X m_{14}
10	1 m_8	m_9		1 m_{11}	m_{10}

• $J_B = Q'_C X' + Q_C X = Q_C \odot X$

$Q_A \backslash Q_B \backslash Q_C X$		00	01	11	10
00	X m_7	X m_1		X m_3	X m_2
01	1 m_4		m_5	1 m_7	m_6
11	1 m_{12}	m_{13}		1 m_{15}	m_{14}
10	X m_8	X m_9		X m_{11}	X m_{10}

• $K_B = Q'_C X' + Q_C X = Q_C \odot X$

• $J_C = 1$

• $K_C = 1$

- Schematic

