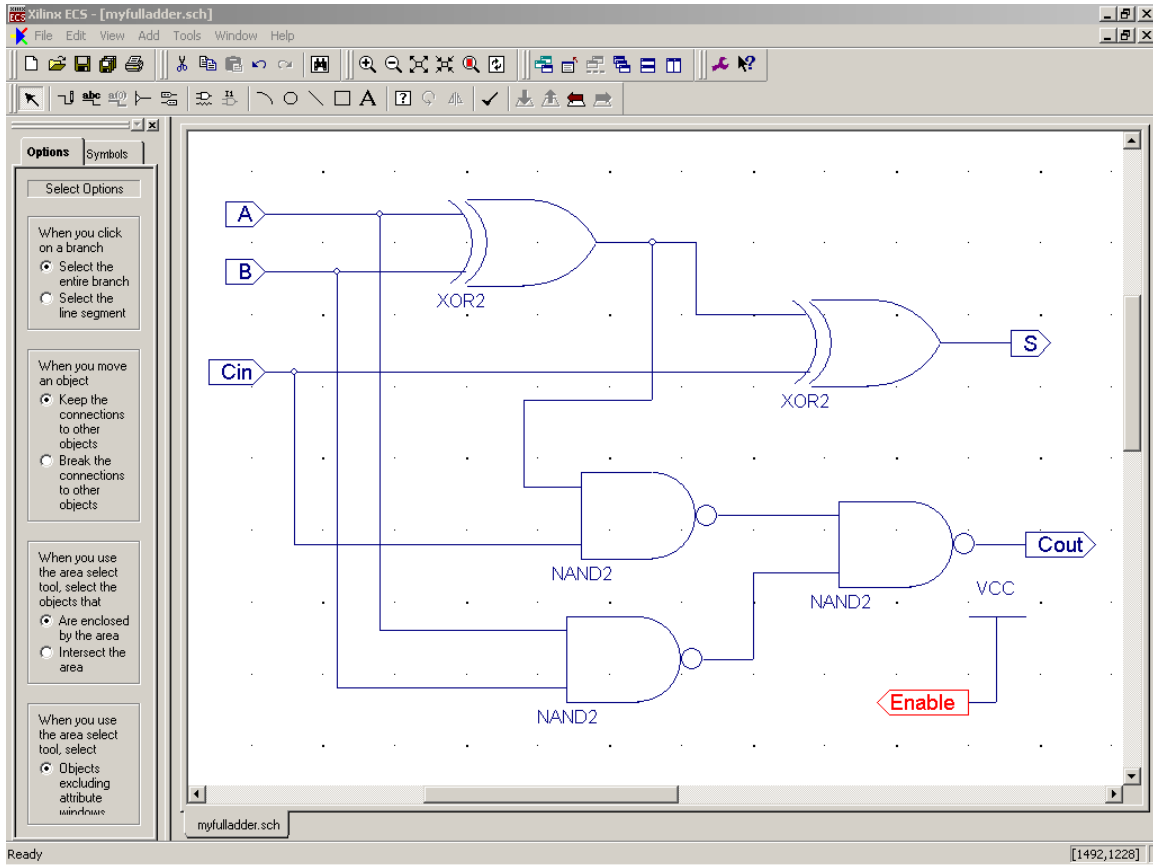


Tutorial to Download
to
Digilab II Board

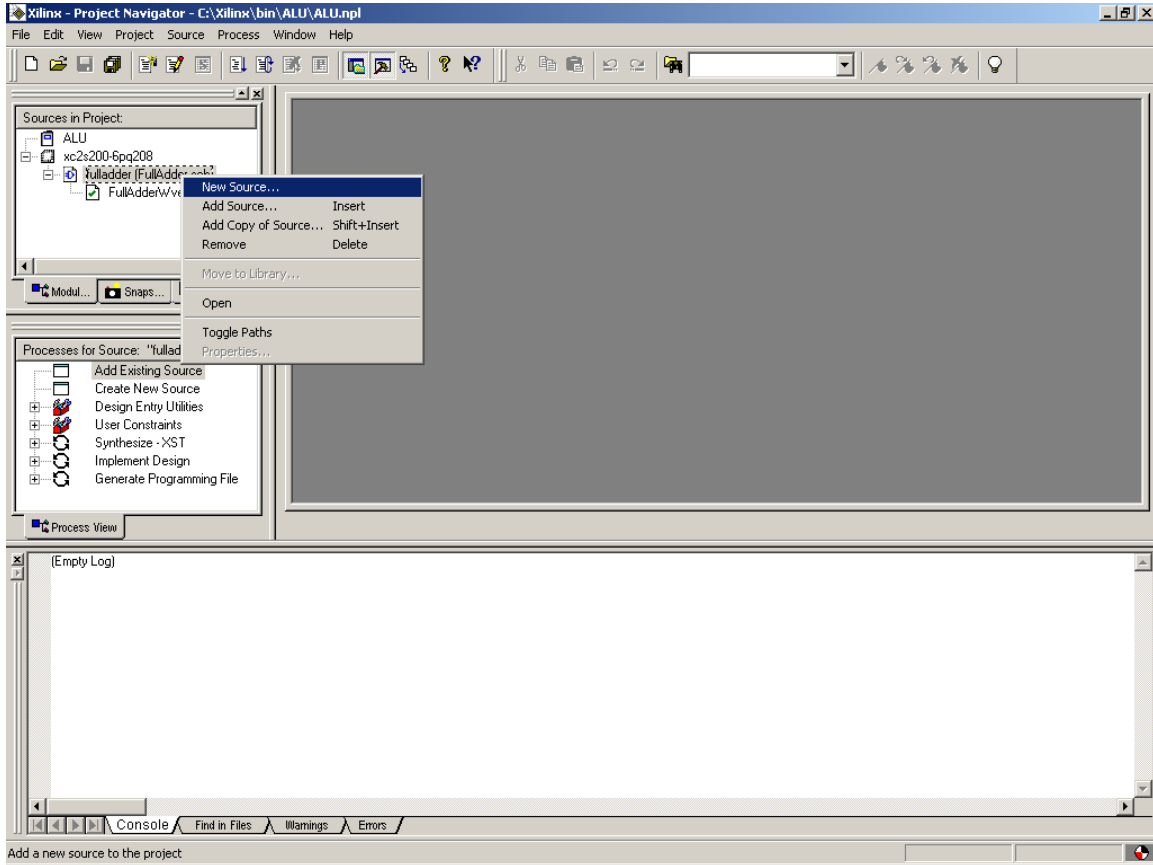
Now that you verified that your design is working, with ModelSIM, it is time to download your design into the FPGA (Field Programmable Gate Array). Let's implement the full adder. On the greatest hierarchy of you design you need to add an extra output. We need to connect Vcc to an output marker.



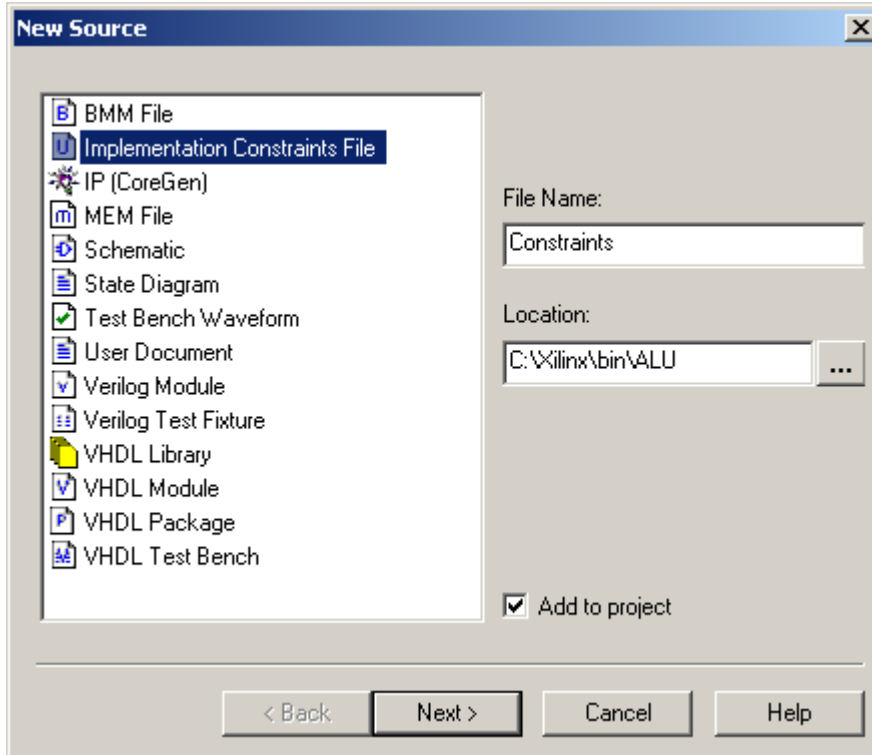
Vcc is located in the **General** category. This extra step is required to enable the LEDs on the board, therefore lets name the output Enable. Save your schematic and return to the Project Navigator.

Before proceeding, once again make sure that the device properties are accurately entered for the target FPGA (Refer page 1 of Xilinx VHDL tutorial)

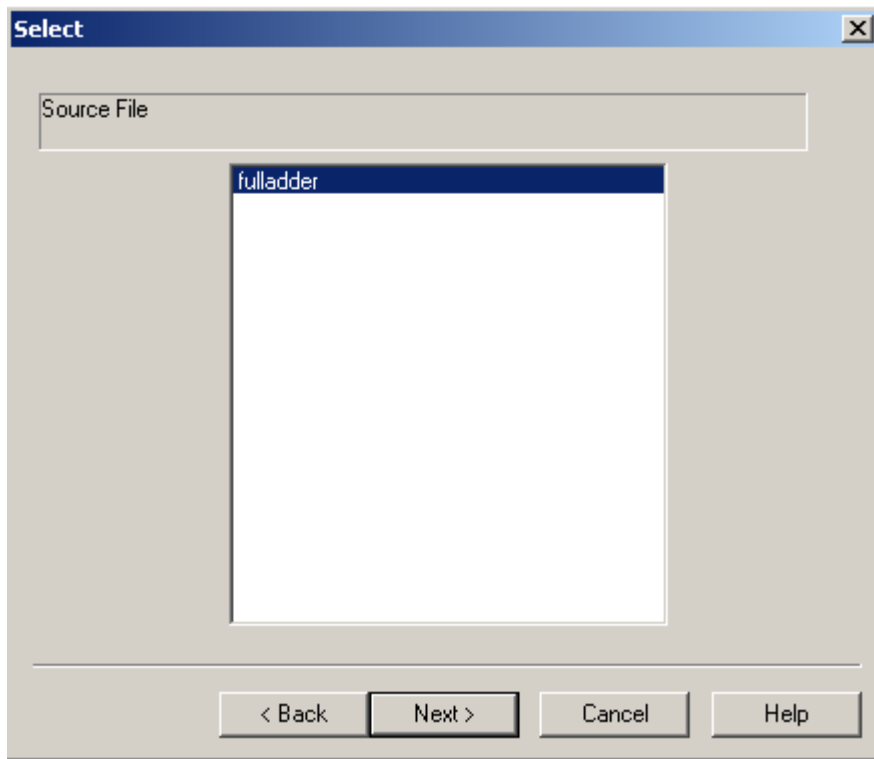
Now from the Project Navigator right click on the schematic to be downloaded and select New Source



This will open a dialog box, prompting you to enter a choice. Select Implementation Constraints File, enter a File name and click Next>

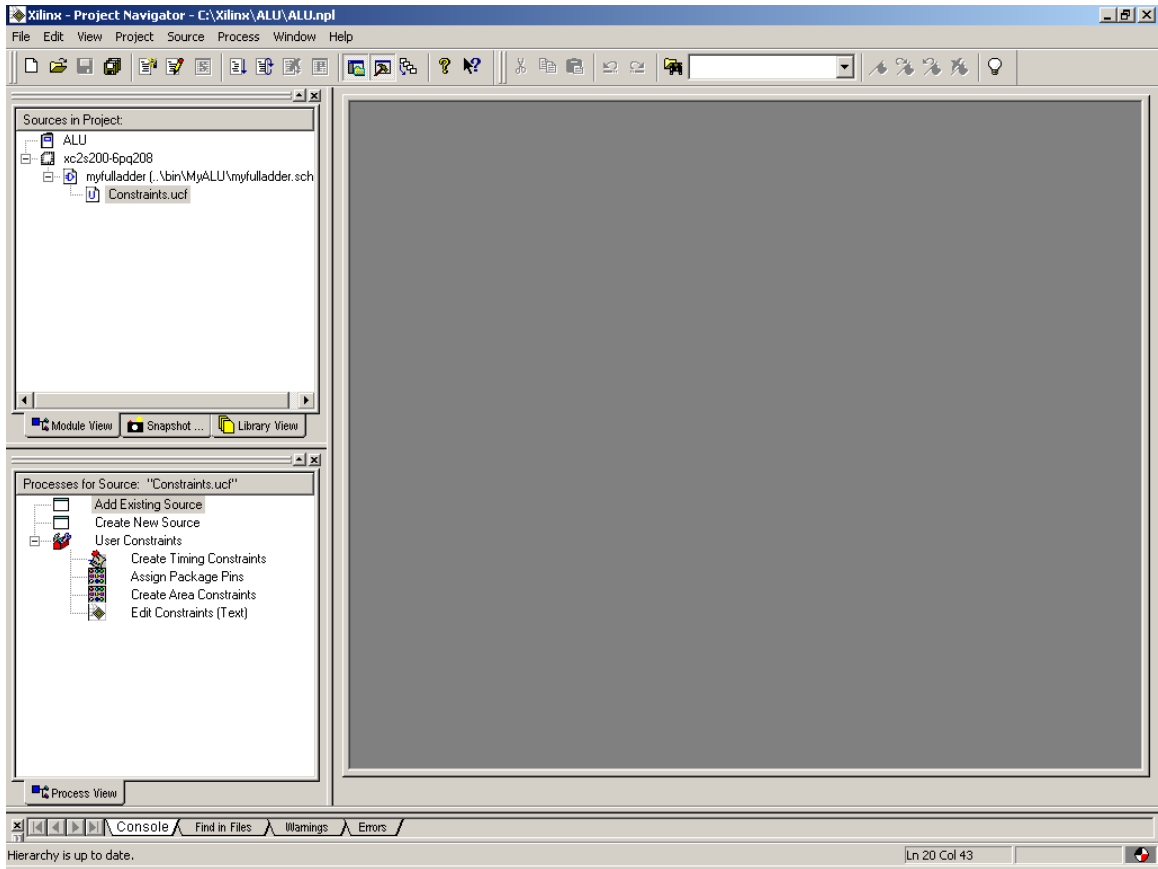


This opens up the following dialog box in which select the appropriate source for which the constraints file is being created.



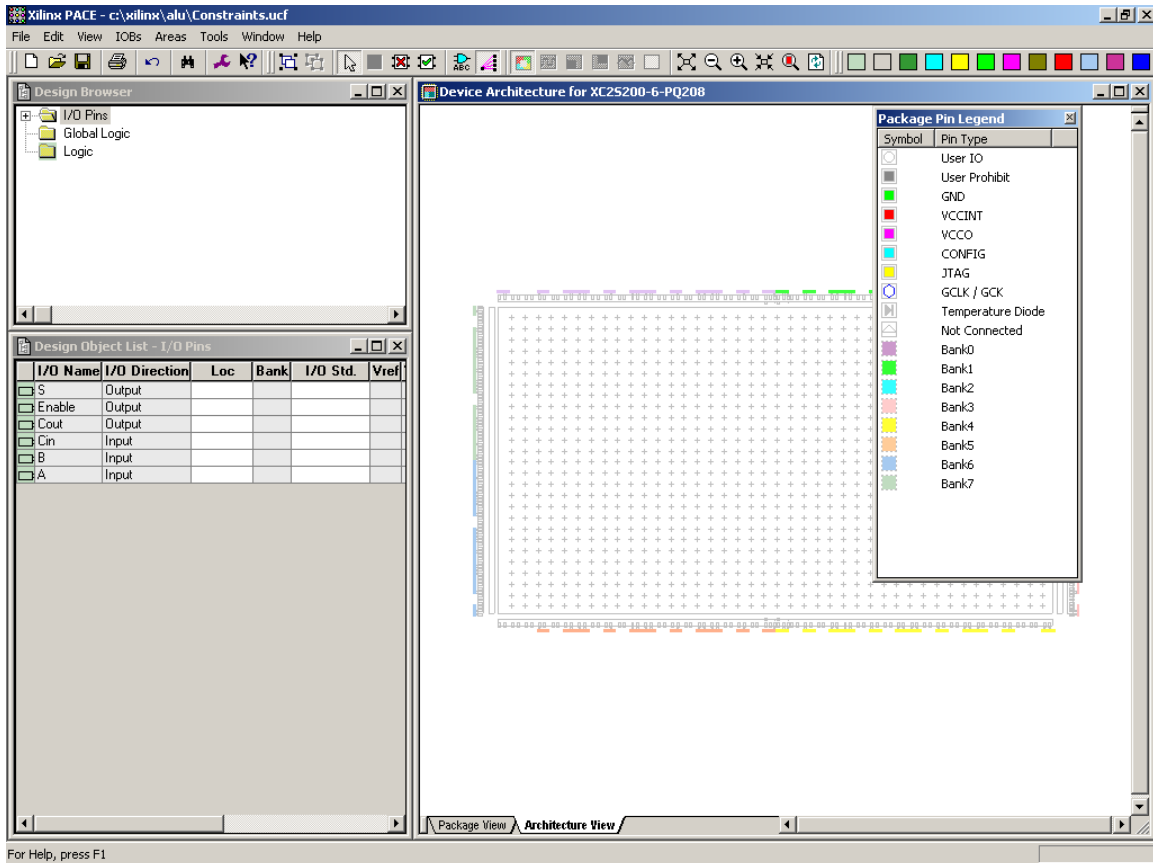
Click Next! And then Finish!

The constraints file, constraints.ucf has been created



Double click on it !

This opens up the Constraints Editor. In the *Design Object List – I/O Pins* window, assign the pin numbers for the inputs (A, B, Cin) and the outputs (S, Cout and enable)



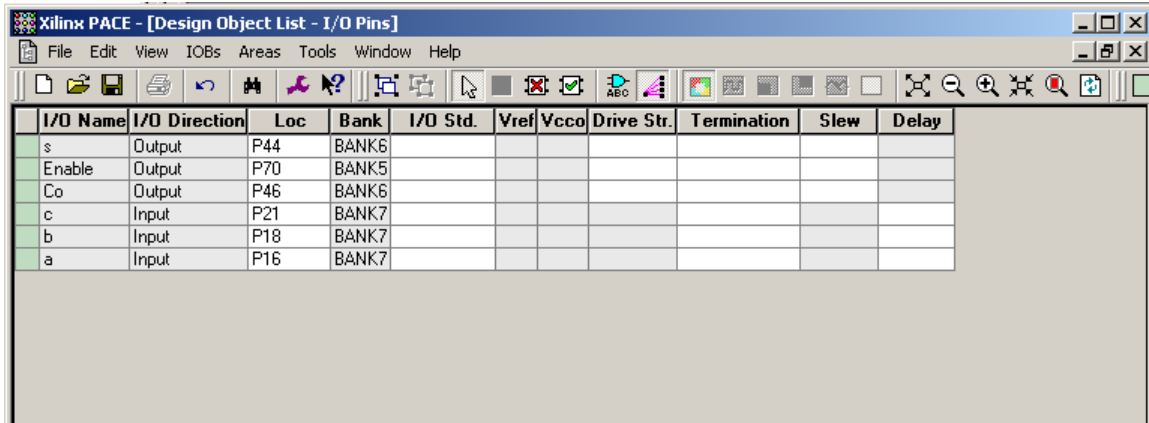
In this window we will assign the Locations of our inputs and outputs to the pins of the FPGA. (See Interconnect Table - Dio1B to D2).

The three inputs (A, B, Cin) need to be assigned to switches. Lets pick the first three switches. The locations of the first three switches (SW1, SW2, SW3) are at locations P16, P18, P21 respectively.

The two outputs (S, Cout) need to be assigned to LEDs. Lets pick the first two LEDs. The locations for the LEDs (LD1 and LD2) are P44 and P46.

The output Enable needs to be assigned to P70 for every project.

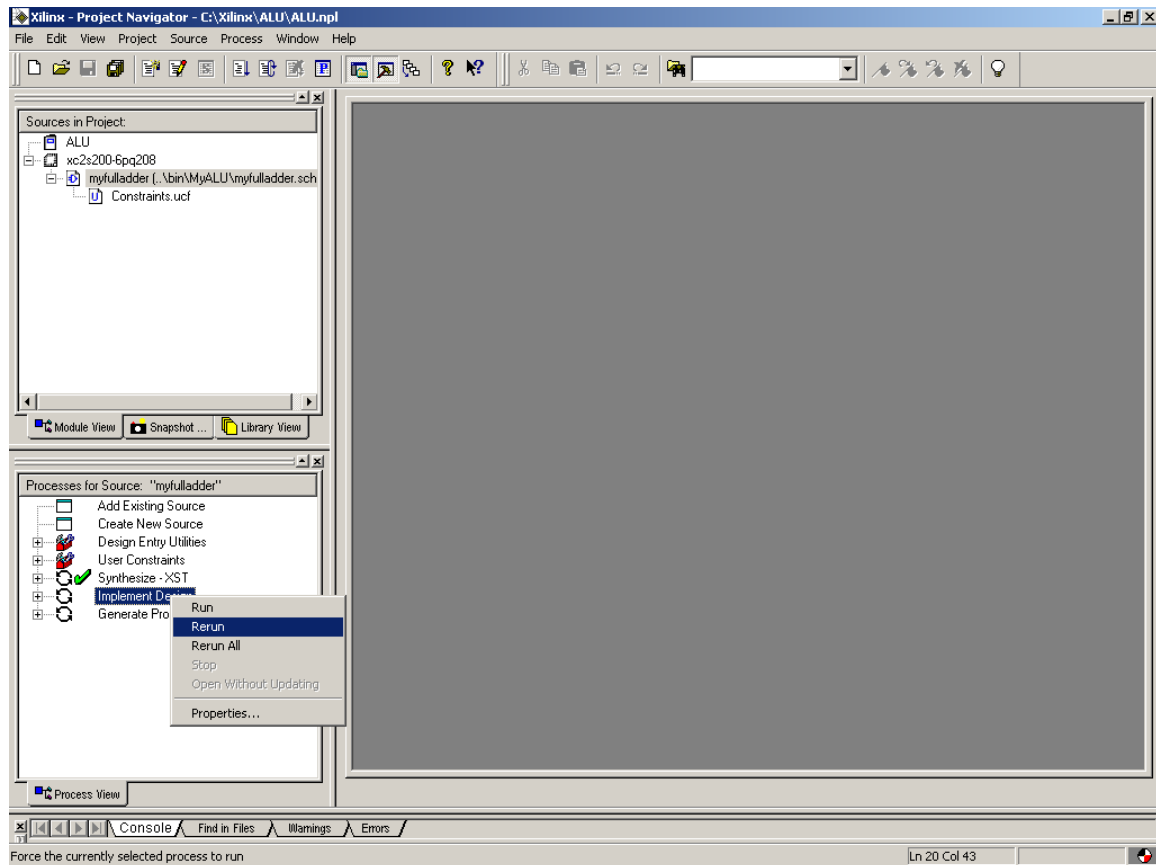
Enter these values into the Locations field of the Constraints Editor. As seen below.



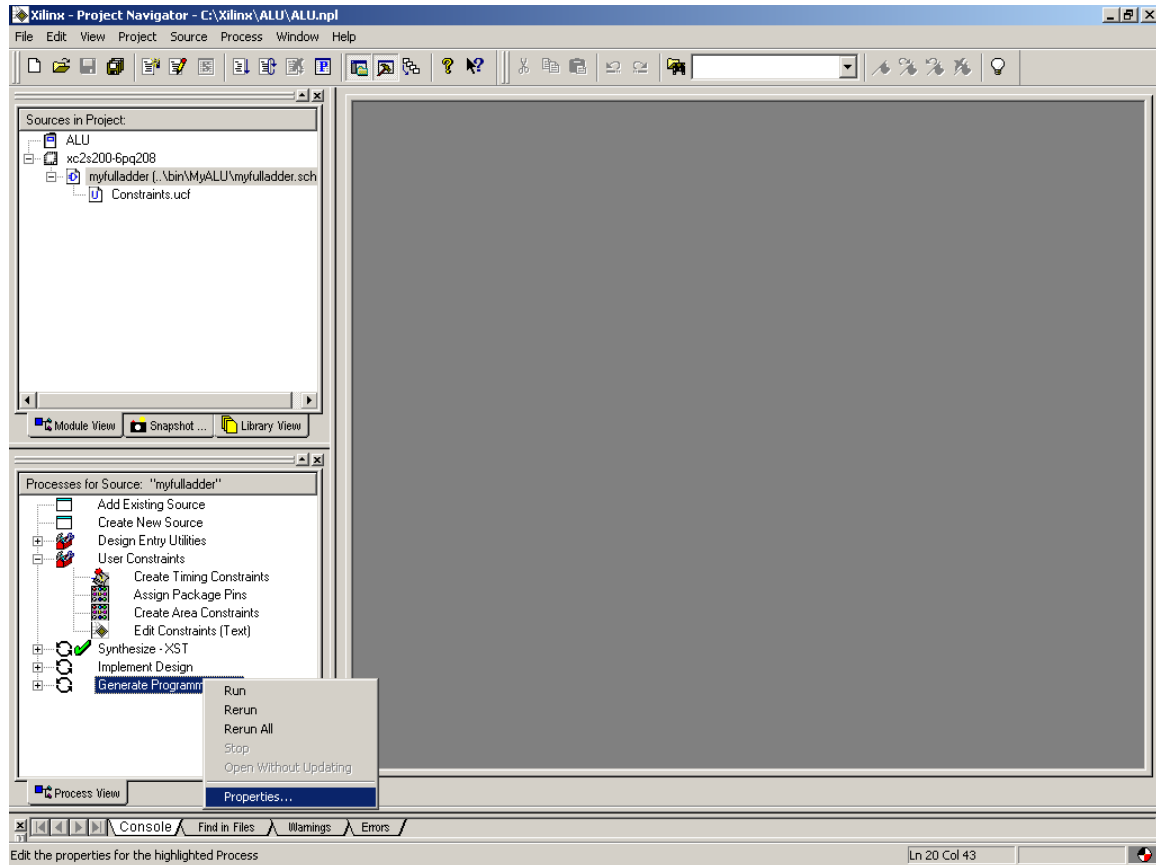
I/O Name	I/O Direction	Loc	Bank	I/O Std.	Vref	Vcco	Drive Str.	Termination	Slew	Delay
s	Output	P44	BANK6							
Enable	Output	P70	BANK5							
Co	Output	P46	BANK6							
c	Input	P21	BANK7							
b	Input	P18	BANK7							
a	Input	P16	BANK7							

Save the changes and close. Return to the project navigator.

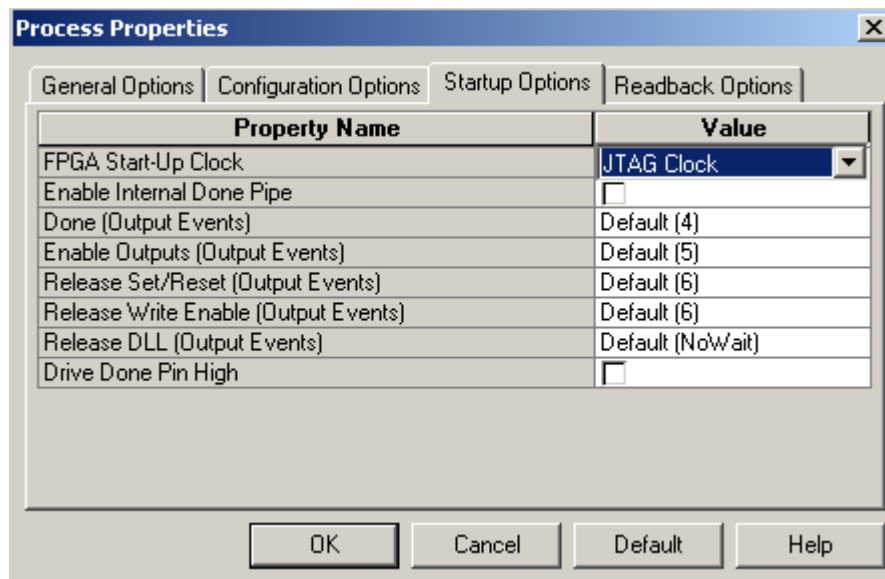
Right click on Implement Design -> Rerun.



If there are no errors generated the next step is to create a BIT file. Right click on Generate Programming File -> Properties.

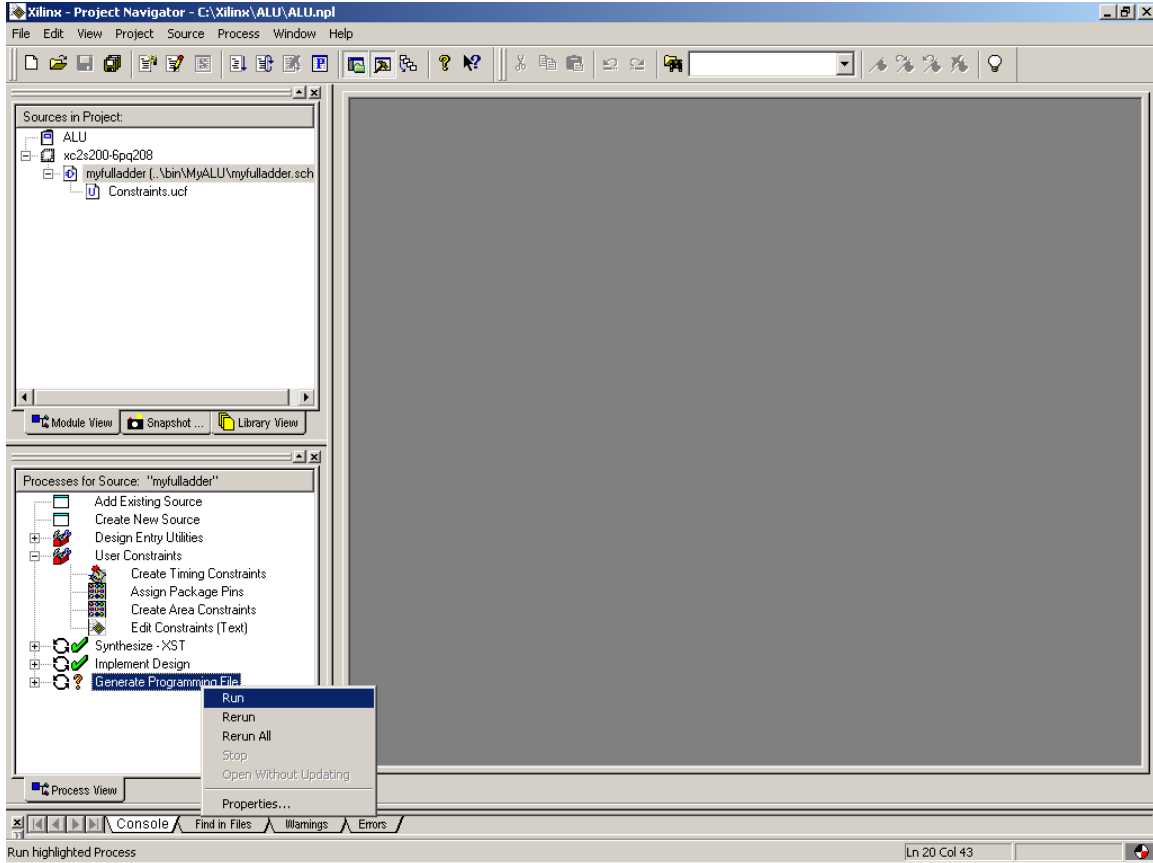


Click the Startup Options tab. And change the Start-Up Clock to JTAG Clock.



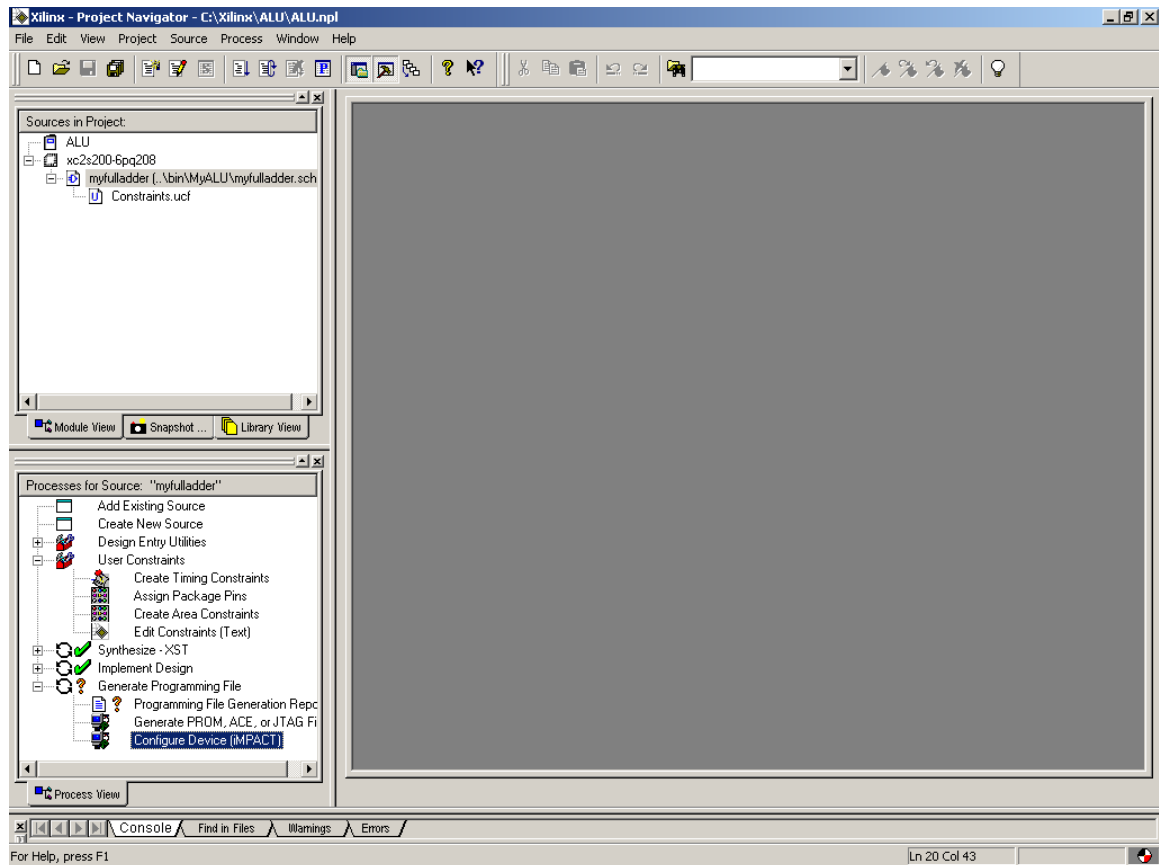
Click Ok.

Right click on Generate Programming File -> Run.

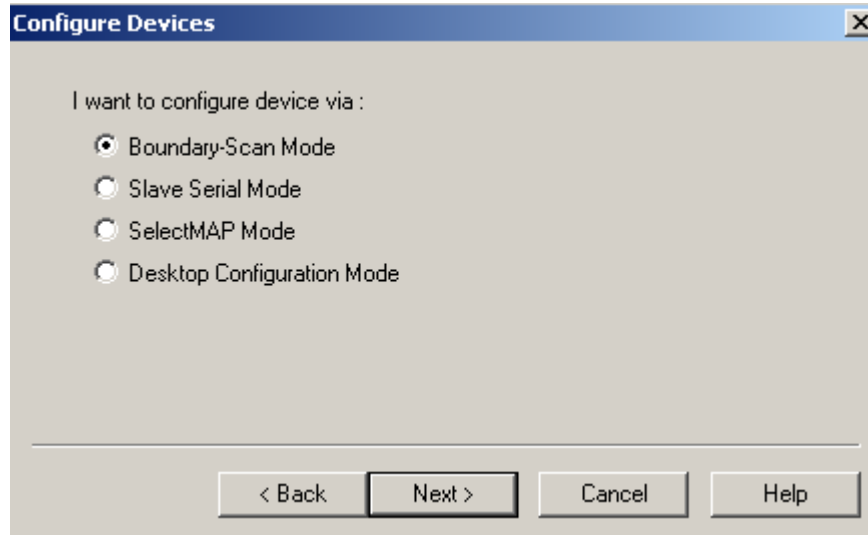


Now your BIT file is ready to be downloaded to the Digilab 2 board.

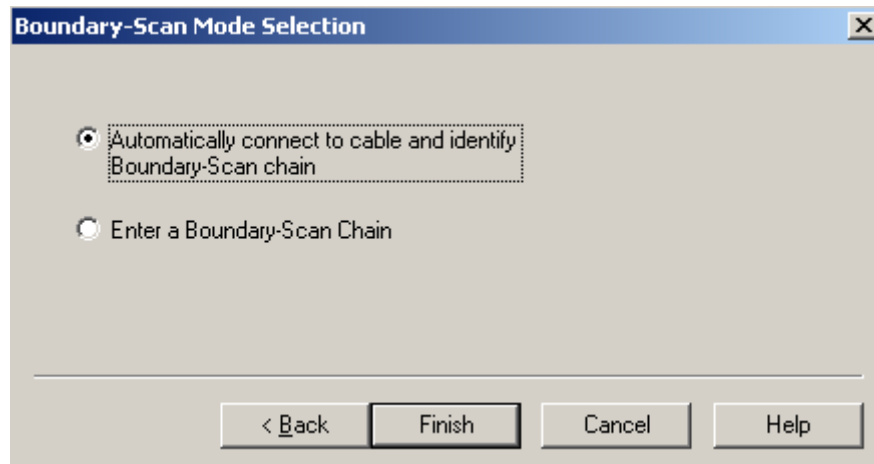
Make sure that the DIO1 board (the smaller one) is connected into tabs E & F of the Digilab 2 board (the larger one). Connect the power supply to the board before you plug the supply to the outlet. Once the Supply is connected and powered up, connect the parallel port to the computer first, then to the board. There is a small switch next to the parallel port on the board. The switch must be in the JTAG position. If it is not in this position then Xilinx will not find the board. Now that everything is connected it is time to download. Return to the Project Navigator. Double click Generate Programming File -> Configure Device (iMPACT)



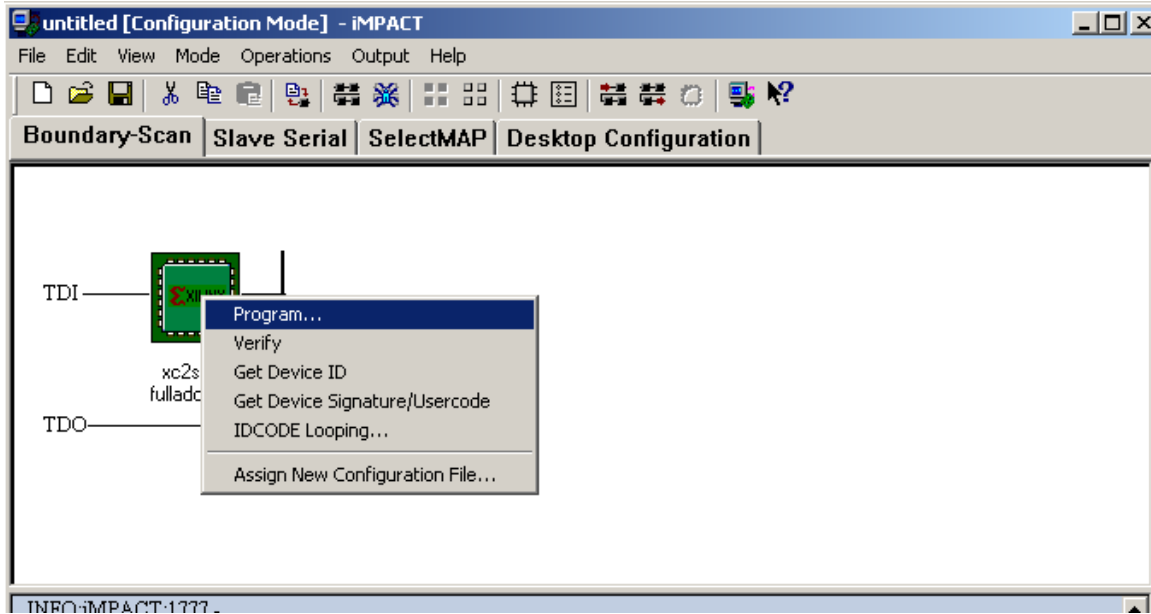
This will open up the following dialog box , Select Configure Devices and Click Next !



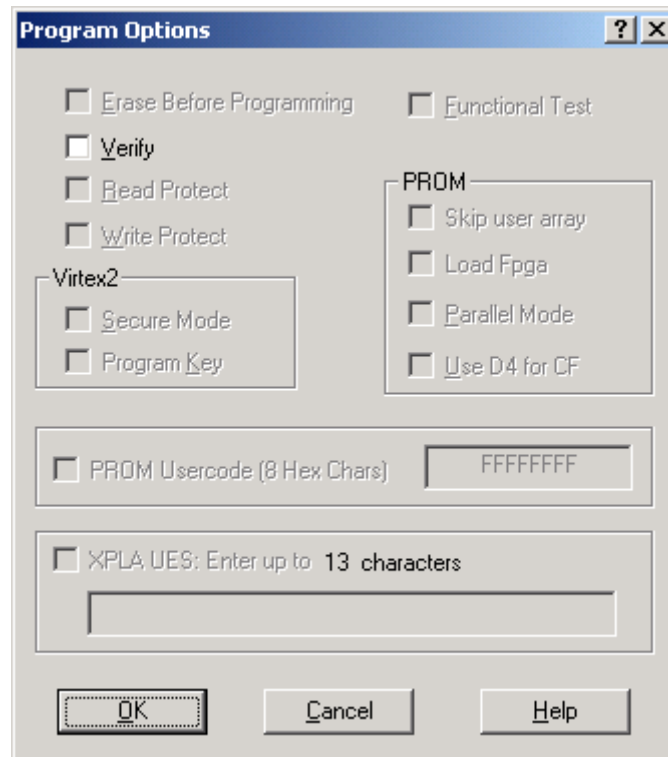
Select **Automatically connect...** in Boundary-Scan Mode Selection and Click Finish.



If the board is not connected properly then it will generate an error saying that it cannot connect to the board. If it finds the board then you can move on.

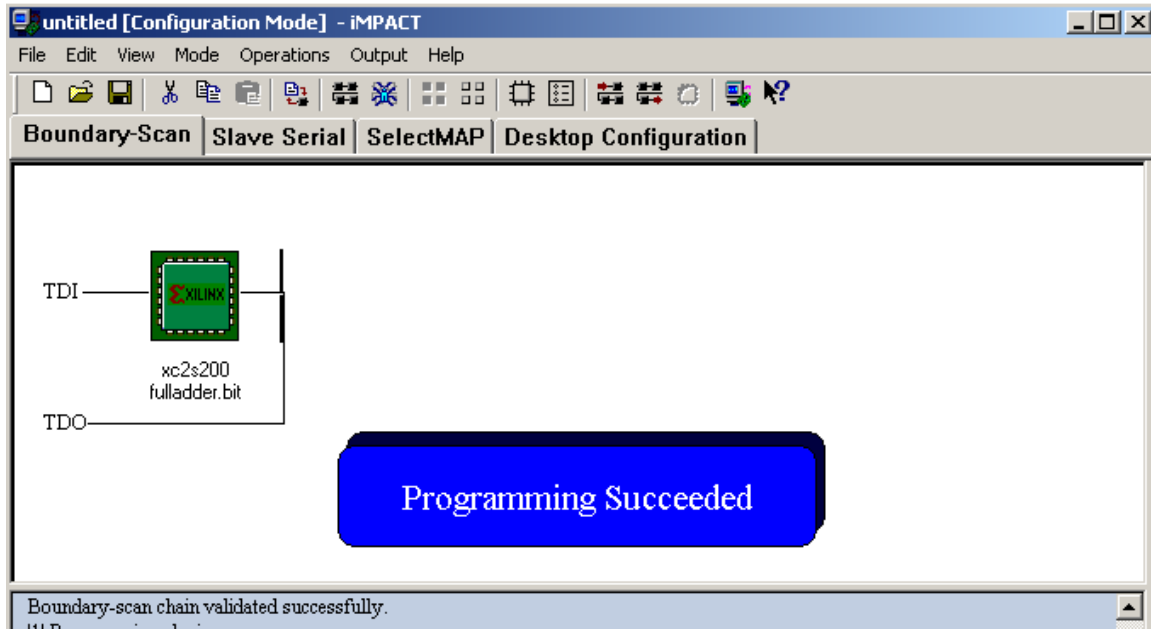


Now right click the picture of the Xilinx chip and select Program...
Select the bite file (*filename.bit*) and click ok.
The following menu will appear.



Click Ok. And the BIT file will begin to download.

If everything was successful the software will show you the following message.



Now flip the switches on the board, and see your design come to life!

SUGGESTIONS FOR ALU

For the ALU we suggest that you use the following switches for each of the 11 inputs.

- *DATA A*

A is a four-bit bus. Therefore, four switches will be needed.

A(3) -> SW1 -> P16

A(2) -> SW2 -> P18

A(1) -> SW3 -> P21

A(0) -> SW4 -> P23

- *DATA B*

B is also a four-bit bus.

A(3) -> SW5 -> P27

A(2) -> SW6 -> P30

A(1) -> SW7 -> P33

A(0) -> SW8 -> P35

- *SELECT LINES*

There are three select lines. We will use the push buttons.

SW(2) -> BTN1 -> P37

SW(1) -> BTN2 -> P41

SW(0) -> BTN3 -> P42

- *OUTPUTs*

There are four data outputs, and four “extra” outputs.

DATA(3) -> LD1 -> P44

DATA(2) -> LD2 -> P46

DATA(1) -> LD3 -> P48

DATA(0) -> LD4 -> P57

Z -> LD5 -> P59

OF -> LD6 -> P61

N -> LD7 -> P63

C -> LD8 -> P68

Digilab Digital I/O 1, Rev B to Digilab D2

DIO1B Pin	Signal	D2 Pin	Signal	FPGA Pin	DIO1B Pin	Signal	D2 Pin	Signal	FPGA Pin
A1		B39			B1	CA	A39	A39	17
A2		B40			B2	SW1	A40	A40	16
A3		B37			B3	CB	A37	A37	20
A4		B38			B4	SW2	A38	A38	18
A5		B35			B5	CC	A35	A35	22
A6		B36			B6	SW3	A36	A36	21
A7		B33			B7	CD	A33	A33	24
A8		B34			B8	SW4	A34	A34	23
A9		B31			B9	CE	A31	A31	29
A10		B32			B10	SW5	A32	A32	27
A11		B29			B11	CF	A29	A29	31
A12		B30			B12	SW6	A30	A30	30
A13		B27			B13	CG	A27	A27	34
A14		B28			B14	SW7	A28	A28	33
A15		B25			B15	DP	A25	A25	36
A16		B26			B16	SW8	A26	A26	35
A17		B23			B17	BTN2	A23	A23	41
A18		B24			B18	BTN1	A24	A24	37
A19		B21			B19	BTN4	A21	A21	43
A20		B22			B20	BTN3	A22	A22	42
A21		B19			B21	A1	A19	A19	45
A22		B20			B22	LD1	A20	A20	44
A23		B17			B23	A2	A17	A17	47
A24		B18			B24	LD2	A18	A18	46
A25		B15			B25	A3	A15	A15	49
A26		B16			B26	LD3	A16	A16	48
A27		B13			B27	A4	A13	A13	58
A28		B14			B28	LD4	A14	A14	57
A29		B11	B11	185	B29		A11	A11	60
A30		B12	B12	182	B30	LD5	A12	A12	59
A31	BLU	B9	B9	188	B31		A9	A9	62
A32	PS2D	B10	B10	187	B32	LD6	A10	A10	61
A33	GRN	B7	B7	191	B33		A7	A7	67
A34	PS2C	B8	B8	189	B34	LD7	A8	A8	63
A35	RED	B5	B5	193	B35	BTN5	A5	A5	69
A36	HS	B6	B6	192	B36	LD8	A6	A6	68
A37	VCC	B3	VCC		B37	VCC	A3	VCC	
A38	VS	B4	B4	194	B38	LDG	A4	A4	70
A39	GND	B1	GND		B39	GND	A1	GND	
A40	VU	B2	VU		B40	VU	A2	VU	